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GOSSIPO-4: an array of high resolution TDCs with a PLL control

F. Zappon,^{a,1} M. van Beuzekom,^a V. Gromov,^a R. Kluit,^a X. Fang^b and A. Kruth^b

^a*Nikhef,*

Science Park 105, Amsterdam, The Netherlands

^b*Bonn University,*

Sigmund-Freud-Str. 25, Bonn, Germany

E-mail: fzappon@nikhef.nl

ABSTRACT: GOSSIPO-4 is a prototype chip featuring an array of high resolution Time to Digital Converters with a PLL control that has been taped out the 9th of August 2011. This prototype is the successor of GOSSIPO-3 test chip and the precursor of the 65k pixel chip TimePix3. The prototype is being developed to test a set of new features that will be used in TimePix3, including a 8 pixel structure sharing one fast oscillator with a new topology, a PLL to provide the control voltage to the oscillators, a custom fast counter and a new small-area cell library.

KEYWORDS: Front-end electronics for detector readout; CMOS readout of gaseous detectors; Particle tracking detectors (Gaseous detectors); Micropattern gaseous detectors (MSGC, GEM, THGEM, RETHGEM, MHSP, MICROPIC, MICROMEGAS, InGrid, etc)

¹Corresponding author.

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1 Introduction

Micro Pattern Gas Detectors (MPGD, see figure 1) consist of a gas volume, that acts as detector medium, and a readout pixel chip. A particle passing through the detector ionizes the gas along its track: the generated electrons drift toward the anode by means of an electric field; close to the readout pad a structure, called InGrid, is biased at high voltage and provides the required amplification so that the charge produced by the ionizing particle can be detected.

The main advantages of this kind of detector are that there is no leakage current due to the sensor and that the input capacitance is very low (less than 10 fF) which result in a very low noise input stage. The grid on top of the chip provides a high gas amplification factor which allows a high single electron efficiency for this type of detector. The use of MPGDs gives the possibility to perform a 3D reconstruction of a particle's track; to do this one needs information about the three coordinates: while the X-Y information is provided by the pixel structure of the readout chip, to recover the Z coordinates measurement of the drift time is necessary. Currently, TimePix chip is used [1]. However, this chip has some limitations: in particular it doesn't allow to record the Time of Arrival (ToA) and the Time over Threshold (ToT) at the same time and, in addition, the available time resolution is not enough for InGrid applications. As an example, consider figure 2 where it is possible to see the ionization track left behind by a particle passing through a GridPix detector with a drift region of 1.8 cm in perpendicular direction. On the bottom plot, we put the track left when the drift region is reduced to 0.1 cm. It is clear that it is not possible to perform a good track fit in this latter case case, having only a few measurements in the data.

Hence, this leads to the necessity to have a time resolution that is on the order of a nanosecond. A series of GOSSIP (Gas On Slimmed Silicon Pixel) chips has been produced to characterize the main components needed to achieve such performance [2]. In this article we will explain how we

Figure 1. Artistic impression of a particle passing through a Micro Pattern Gas Detector. Courtesy of M. Fransen.

Figure 2. Test beam event; on the top and on the bottom it is possible to see the electrons released in two GridPix detectors by a perpendicular incoming particle. The two detectors have a different size of the amplification region. Courtesy of W. Koppert.

perform time measurements and we will give an overview of the main results coming from the test of GOSSIPO-3 [3]. Then we will describe GOSSIPO-4, focusing on the reasons behind this new prototype and the simulations results.

Figure 3. Timing diagram used in GOSSIPO-3 and GOSSIPO-4.

2 Time measurements

The main scheme used to perform time measurements is visible in figure 3.

When the signal goes above threshold a fast oscillator (640 MHz) is started and it is stopped by the first rising edge of the system clock (40 MHz): the number of oscillations is recorded in the Fast Counter and provides the required resolution. After this, the number of system clock cycles is recorded in the Slow Counter until a Trigger signal arrives (common stop) synchronous with the system clock; the combination of the Fast Counter and the Slow Counter gives the ToA of the particle. It is then straightforward to add to this structure another counter to record the ToT: this counter starts counting system clock cycles at the same moment as the Slow Counter and it stops when the signal goes below threshold.

3 GOSSIPO-3: test results

GOSSIPO-3 is a prototype chip developed in collaboration between Nikhef and Bonn University. It contains two pixels, one equipped with a full analog frontend while the other has only the digital components (state machine and counters, see figure 4). Tests of the chip proved the functionality of the analog frontend, the foreseen characteristics of the Low Drop Out regulators and, in general, the reproducibility of the characteristics across different chips.

To characterize the Time to Digital Converter (TDC) we injected a pulse at the input of the pixel and delayed it with respect to the Trigger: an example of the outcome of such test is presented in figure 5. In this figure it is possible to notice the difference in size between bin 1 and bin 2. As a side note, notice that bin 0 is not taken into account in the analysis: this bin is intentionally smaller than the others. The choice comes from the fact that the counters are Linear Feedback Shift Registers. This means that with the 4 bits available for the Fast Counter we can obtain only 15 different counting values. Given that the system clock frequency has been chosen to be 40 MHz (period of 25 ns) and the oscillator runs with a period of 1.65 ns we are left with fractions of nanosecond.

Figure 4. Block diagram of the analog pixel of GOSSIPO-3. Notice that the oscillator is present in each pixel.

Figure 5. An example of the test results performed in GOSSIPO-3: notice the large difference in bin size, in particular bin 1 with respect to the other bins.

Table 1. Analysis results of Chip 1 for the full pixel (analog) and the only digital. Notice the big DNL. The value in brackets refers to the DNL calculated not taking into account bin 1.

Chip	Bin size (ns)	Error	Jitter (ns)	Error	DNL
1 Digital	1.7525	0.3217	0.052	0.052	19.90%
1 Analog	1.7701	0.2163	0.09	0.01	31.83% (19.90%)

The important aspect to notice is highlighted in table 1: a big Differential Non Linearity in the TDC characteristic is present, most likely caused by a crosstalk from the system clock. The effect, though, is not fully reproducible in simulations.

4 GOSSIPO-4: design

Given the results shown in section 3 a new design has been planned in the framework of the TimePix3 chip. To overcome the above mentioned problems, GOSSIPO-4 uses a 8 pixel struc-

Figure 6. Schematic of the oscillator used in GOSSIPO-4.

Figure 7. Variation of the oscillation period for different values of VDD and Vcntr. Notice the plateau, indicating stable operations, for VDD > 1.2 V.

ture that shares a voltage controlled oscillator in contrast with GOSSIPO-3 where each pixel has his own oscillator. In addition, the topology of the oscillator has been changed to be less sensitive to any effect on the supply voltage, which is most likely the main source of the effects we see in GOSSIPO-3. A Phase Locked Loop (PLL), which contains a replica of the oscillator, is placed in the periphery of the chip and provides the required control voltage to keep the oscillation frequency locked to 640 MHz. Additionally, four rail-to-rail buffers have been placed to be tested. The chip is 1x2 mm and it contains 30 Super-Pixel for a total of 240 pixels.

4.1 Oscillator

In GOSSIPO-4 the four-stage ring oscillator has been redesigned to be less sensitive to variation of the supply voltage as this seems to be the main cause of the non-linear effects we see in GOSSIPO-3. In figure 6 you can see the schematic: notice that the power supply and the control voltage (Vcntr) are separated.

This latter voltage is provided by a PLL that has in it a replica of the oscillator and it is used to mitigate effects due to process and temperature variations. The channel-to-channel mismatch is foreseen to be of the order of 0.4% in the TT corner. In figure 7 is shown the variation of the oscillation period as function of VDD for various values of the control voltage. It is important to notice that for VDD > 1.2 V the frequency is independent of the Supply voltage over a wide range of control voltages.

Figure 8. Block diagram of the super pixel structure adopted in GOSSIPO-4. The oscillator is shared among 8 pixels to save area and to reduce the power consumption.

4.2 Super Pixel

To save area and to reduce the power consumption it has been decided to adopt a new structure called Super Pixel (see figure 8). The concept is based on sharing one oscillator among 8 pixels, distributing the fast clock to all of them. If a pixel is hit the oscillator is started and the number of oscillations is recorded in its Fast Counter; then, if a second pixel in the group is hit, the Fast Counter of this second pixel simply records the number of oscillations from that moment to the first rising edge of the system clock when the oscillator is stopped. This operation of synchronizing the asynchronous signal, as the one coming from the detector, to the already running clock is performed inside the pixels by a special block called Synchronization Logic (see section 4.3).

4.3 Pixel

In figure 9 you can see the block diagram of the GOSSIPO-4 pixel. The two most important structures are the custom designed Fast Counter and Synchronization Logic. These two blocks have been custom designed because we need to be sure that they meet specifications and work properly, since they are the key components in achieving the high precision time measurements. In fact, early stage simulations have shown metastability problems occurring when using standard cells: in particular, the simultaneous switching of the fast clock and the system clock could lead to an unpredictable state in the counter; moreover the blocks are running at the limit speed for the technology. The two blocks together occupy roughly the 12% of the pixel area (Counter and Synchronization Logic take respectively $179.52 \mu\text{m}^2$ and $187.11 \mu\text{m}^2$).

In the pixel are present several structures that have been placed only for test purposes. At the input there is a multiplexer to be able to select among four different time independent test signals: this gives us the possibility to completely characterize the super pixel and its behavior in response to different stimuli. At the output we decided to adopt a simple solution using a serial readout.

5 Conclusion

In the framework of TIMEPIX-3 chip a new prototype chip called G4 has been designed and submitted to test the reliability of a new structure to perform high precision time measurements. In particular, we hope to eliminate the effects we see in GOSSIPO-3: we have changed the topology of the Oscillator to be less sensitive to effects that might be caused by variations in the supply voltage. Moreover, by means of a custom designed Synchronization Logic and Fast Counter, we should guarantee a metastability free structure, an issue that is present in synchronization circuits and that has been highlighted by early-stage simulations. The chip has been submitted at the beginning of August 2011 and will be tested to prove the solidity of the proposed solution in view of an integration in TIMEPIX-3.

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