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Shen, Y.; Niknam, S.; Pathania, A.; Pimentel, A.D.

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Thermal Management for S-NUCA Many-Cores via Synchronous Thread Rotations

Yixian Shen, Sobhan Niknam, Anuj Pathania, and Andy D. Pimentel
University of Amsterdam, Amsterdam, The Netherlands
y.shen@uva.nl, s.niknam@uva.nl, a.pathania@uva.nl, a.d.pimentel@uva.nl

Abstract—On-chip thermal management is quintessential to a thermally safe operation of a many-core processor. The presence of a physically distributed logically shared Last-Level Cache (LLC) significantly reduces the performance penalty of migrating threads within the cores of an S-NUCA many-core. This cost reduction allows novel thermal management of these many-cores via synchronous thread migration. Synchronous thread migration provides a viable alternative to Dynamic Voltage and Frequency Scaling (DVFS) and asynchronous thread migration used traditionally to manage thermals of S-NUCA many-cores.

We present a theoretical method to compute the peak temperature in many-cores with synchronous thread migrations. We use the method to create a thermal management heuristic called HotPotato that maximizes the performance of S-NUCA many-cores under a peak temperature constraint. We implement HotPotato within the state-of-the-art HotSniper simulator. Detailed interval thermal simulations with HotSniper show an average 10.72% improvement in response time of S-NUCA many-cores when scheduling with HotPotato compared to a state-of-the-art thermal-aware S-NUCA scheduler.

I. INTRODUCTION

Many-core processors house tens of cores on a single die and excel in executing multi-threaded applications with significant inter-thread communication [1]. In shared memory many-cores, the cores (overlying threads) communicate indirectly using a logically shared memory address space. The cores can always communicate with each other using the off-chip main memory. However, to minimize the communication cost (latency), many-cores come with a low-latency on-chip Last-Level Cache (LLC). LLC itself is often physically distributed between the cores as cache banks to distribute the on-chip cache coherency traffic. The banks are connected using a Network-on-Chip (NoC) to allow for a bottleneck-free flow of traffic [2].

Static Non-Uniform Cache Architecture (S-NUCA) is a memory architecture that statically maps the LLC to the main memory [3], [4]. S-NUCA allows for a quick search for a cache line (page), given the static mapping with minimal cache coherence. During a thread migration on an S-NUCA many-core, only the cache lines stored in private caches on the core from where the thread migrates need flush to the LLC. The shared LLC then refills the cache lines on another core where the migrated thread restarts its execution. Consequently, the physically distributed logically shared LLC and an NoC significantly reduces the cost of thread migrations on many-cores with S-NUCA caches.

S-NUCA many-cores, similar to other many-cores, suffer from thermal issues [5]. Thermal-aware schedulers primarily depend upon Dynamic Voltage and Frequency Scaling (DVFS) technology to manage the thermals for S-NUCA many-cores [6]. DVFS reduces a core’s frequency (and voltage) to reduce its power consumption and lower its temperature [7], [8]. However, DVFS also results in a significant drop in the performance of the overlying applications [9]. Thermal-aware schedulers also incorporate thread migrations as an additional knob to prevent hotspots from forming on-chip on S-NUCA many-cores [10]. However, schedulers perform these migrations asynchronously on-need basis and often as a measure of last resort. These on-demand asynchronous thread migrations combined with DVFS represent the state-of-the-art strategy for thermal-aware schedulers for S-NUCA many-cores.

The task migration penalty for S-NUCA is not particularly severe because the LLC cache in S-NUCA is logically shared and physically distributed. Therefore, only the private L1 and L2 caches require a refresh on migrations. In this work, we make an observation that the average performance penalty from thread migrations is significantly lower than DVFS on S-NUCA many-cores. Based on this observation, we propose a novel method for thermal management for S-NUCA many-cores that involves synchronously rotating (migrating) threads on S-NUCA many-cores such that no core has a chance to heat up beyond the given thermal threshold. Synchronous task rotations average the temperatures between hot and cold cores, allowing us to investigate the periodic solution for thermal management of S-NUCA many-cores.

Motivational Example. Figure 1 shows an abstraction of a 16-core S-NUCA many-cores. In this example, we primarily focus on the center-most cores of the many-core, namely Cores 5, 6, 9, and 10. We simulate the many-core using detailed interval thermal simulations using the HotSniper [12] toolchain. We set the thermal threshold at 70 °C.

Figure 2(a) shows the thermal trace when a two-threaded blackscholes benchmark from PARSEC [13] benchmark suite executes on Cores 5 and 10 of the many-core running at their peak frequency of 4GHz. This execution results in a

Fig. 1: Synchronous thread rotation on a S-NUCA many-core.
We are the first to propose thermal management for S-NUMA many-cores using synchronous thread migrations. We propose (based on the underlying many-core thermal model [15]) an analytical method for calculating the peak temperature of a synchronously rotating sequence of threads on a set of cores at a certain rotation frequency. We integrate the method into a run-time scheduler called HotMig that selects a performance-maximizing thermally-safe rotation on S-NUMA many-cores. We implement HotMig in the state-of-the-art HotSniper simulator. We show the superiority of HotMig over a state-of-the-art thermal-aware scheduler for S-NUMA many-core using detailed interval thermal simulations.

Open-Source Contributions. The source code for the HotMig scheduler as a HotSniper plugin is available for download at https://github.com/yixianuva/hotpotato.

II. RELATED WORK

The authors of [16] were the first to propose thread (task) rotation to mitigate the peak temperature of single-core processors. They heuristically calculated the sequence of single-threaded kernels that run to completion sequentially such that the peak temperature of a single-core processor minimizes. The heuristic relies on chaining hot and cold threads in the execution sequence to minimize peak temperature. However, the complexity of the involved optimization problem increases significantly from a single-core to many-core, executing multiple multi-threaded tasks in parallel.

Authors of [3] were the ones to introduce S-NUMA memory architecture. Subsequently, several S-NUMA many-cores made it to the market [17]. However, like other many-cores, S-NUMA many-cores also suffer thermal issues [5], [18]. Therefore, their thermal management remains an active research subject. Authors of the [19] were the first to characterize the performance heterogeneity in cores of an S-NUMA many-core due to the presence of physically distributed LLC and NoC. Authors of [6] were the first to combine the performance heterogeneity and thermal heterogeneity in cores of S-NUMA many-cores for their thermal management.

In [6], [20], the authors present a DVFS-based thermal-aware scheduler called PCGov that uses TSP-based [14] power-budgeting for mapping tasks on S-NUMA many-cores. Authors of [10], [21] present a thermal-aware scheduler called PCMig that extends PCGov with neural network-driven asynchronous
on-demand thread migrations. PCMig, to the best of our knowledge, remains the state-of-the-art thermal-aware scheduler for S-NUCA many-cores. In this work, on S-NUCA many-cores, we show HotPotato, with its synchronous thread migration (without DVFS), is superior in performance to PCMig with its DVFS and asynchronous on-demand thread migrations.

III. SYSTEM MODELS

A. Architecture Model

Figure 1 contains the abstraction of the architectural model used in this work. The target architecture is an S-NUCA many-core with $n$ micro-architecturally homogeneous cores. A grid-based NoC employing XY-routing connects the cores. Each core holds a bank of the physically distributed logically shared L2 LLC. Each core also has a private L1-Instruction and Data cache and an NoC-router. The performance (or thermals) of cores is positively (or negatively correlated) to their Average Manhattan Distance (AMD) from other cores [19]. The topography of the many-core dictates that the AMD of the cores increase as we traverse away from the many-core’s center.

B. Thermal Model

We employ a well-known RC thermal model based on the duality between thermal behavior and electrical circuits [15]. RC thermal model has $N$ thermal nodes wherein the first $n$ nodes represent the $n$ cores of the many-core, and the remaining $N - n$ nodes correspond to the cooling system. As per the model, we can compute the temperature of each thermal node (a function of its power consumption, the temperature of neighboring thermal nodes, and the ambient temperature) by a set of $N$ first-order differential equations.

\[ AT' + BT = P + T_{amb}G \]  

where $A = [a_{i,j}]_{N \times N}$ contains the thermal capacitance values of each thermal node, $B = [b_{i,j}]_{N \times N}$ represents the thermal conductivity values between neighboring nodes, $T = [T_i(t)]_{N \times 1}$ denotes the temperature on every node at time instant $t$, $T' = [T_i(t)]_{N \times 1}$ accounts for the first order derivative of the temperature on each node concerning time, $P = [p_i]_{N \times 1}$ contains the power consumption on each node, and $G = [g_i]_{N \times 1}$ contains the thermal conductivity between each node and ambient temperature. By defining matrix $C = -A^{-1}B$, we can rewrite Equation (1) as follows.

\[ T' = CT + A^{-1}P + T_{amb}A^{-1}G \]  

As the temperature of cores approaches the steady state, we can rewrite Equation (1) as follows.

\[ T_{steady} = B^{-1}P + B^{-1}T_{amb}G \]  

where $T_{steady} = [T_{steady_i}]_{N \times 1}$ contains the steady-state temperature of per node and $B^{-1}$ is the inverse of the matrix $B$.

IV. PEAK TEMPERATURE CALCULATION

Thread rotation involves executing threads rotating periodically on thermally-coupled cores of a many-core. We present a computationally-efficient analytical solution to calculate the peak temperature for a given thread rotation on a set of cores. Let $P$ be the power consumption vector of the rotating threads. Due to performance heterogeneity, the same thread can have different power consumption on different cores, and our proof accounts for these differences.

Let the threads execute for a fixed epoch $\tau$ on each core during the rotation. Let $T_{init} = [T_{init_i}]_{N \times 1}$ be the matrix storing the initial temperature of nodes at time $t = 0$. Initial conditions are mandatory for solving the involved differential equations. We use MatEx [22] to solve for the transient temperature via the matrix exponential method. We can obtain the temperature at time $\tau$ as a function of $T_{init}$ using the following equation.

\[ T_\tau = T_{steady} + e^{C\tau}(T_{init} - T_{steady}) \]  

where $P_\tau$ denotes the average power consumption of the rotating threads over the epoch $\tau$, and $I$ is an identity matrix of size $N$. Let $T_{init}$ be the temperature at the end of $\delta$ epochs. The temperature $T_{init}$ is the initial temperature for epoch $(\delta + 1)\tau$. We define $w = (I - e^{C\tau})B^{-1}$ as the rotational factor. The subsequent temperature traces evolves based on Equation (4). Therefore, the temperature $T_{\delta\tau}$ after the first rotation period $\delta$ (or after $\delta\tau$ epochs) is as follows.

\[ T_{\delta\tau} = wP_{\delta\tau} + e^{C\tau}(wP_{(\delta-1)\tau} + \cdots + e^{(\delta-1)C\tau}wP_{\tau}) \]  

The temperature $T_{\delta\tau}$ is a combination of power history over the rotation period $\delta$ and rotation factor $w$. Let $d$ be rotation periods where after the transient temperature pattern in a rotation approaches a steady state and then repeats itself. The first temperature component $T_{(d\delta+1)\tau}$ after $d\delta$ durations is as follows.

\[ T_{(d\delta+1)\tau} = (I + \sum_{i=1}^{d} e^{iC\tau})wP_{\tau} + \sum_{i=1}^{d} e^{(i-1)d\tau}C\tau wP_{\tau} + \cdots + \sum_{i=1}^{d} e^{(i-1)d\tau}C\tau wP_{\tau} \]  

$T_{(d\delta+1)\tau}$, therefore, is a combination of power history and the accumulated rotation component. As per the thermodynamic Equation (4), matrix $A$ is an invertible matrix and $B$ is symmetrical. Therefore, we can factorize matrix $C$. Consequently, we can analytically solve $e^{C\tau} = \cdots$. 

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$[e^{C \tau}]_{N \times N}$ as a matrix exponential using $e^{C \tau} = VDQ^{-1}$, where $V = [v_{i,j}]_{N \times N}$ are the eigenvectors of matrix $C$. Let $D = \text{diag}(e^{\lambda_1 \tau}, e^{\lambda_2 \tau}, \ldots, e^{\lambda_N \tau})$ be the diagonal matrix where $\lambda_1, \lambda_2, \ldots, \lambda_N$ represent the eigenvalues of matrix $C$. The following equation gives the matrix addition after the matrix exponential decomposition for rotational components.

$$\sum_{i=1}^{d} e^{C \tau} = V \cdot \text{diag} \left( \sum_{i=1}^{d} e^{\lambda_1 \tau}, \sum_{i=1}^{d} e^{\lambda_2 \tau}, \ldots, \sum_{i=1}^{d} e^{\lambda_N \tau} \right) \cdot V^{-1} \quad (8)$$

Since $A^{-1} B$ is congruent to identity matrix $I$ [22], it is also a positive definite matrix, so $C = A^{-1} B$ is a negative definite matrix. As a result, eigenvalues are all negative. Therefore, as $d \to +\infty$ in the steady state, the sum of each element in eigenvalues of the diagonal matrix in Equation (8) is given by the following.

$$\lim_{d \to +\infty} e^{\lambda_1 \tau} + e^{\lambda_2 \tau} + \ldots + e^{\lambda_N \tau} = e^{\lambda_1 \tau} + \frac{e^{\lambda_2 \tau}}{1 - e^{\lambda_1 \tau}} \quad (9)$$

Therefore, each element in the diagonal element is upper bounded by a fixed value in the steady state and is independent of $d$. Due to the linear nature of the matrix transformation, we get a safe upper bound of the peak temperature. We can use Equations (8) and (9) to rewrite Equation (7) as the following.

$$T_{(d+1)+} = V \cdot \text{diag} \left( \frac{1}{1 - e^{\lambda_1 \tau}}, \frac{1}{1 - e^{\lambda_2 \tau}}, \ldots, \frac{1}{1 - e^{\lambda_N \tau}} \right) \cdot V^{-1} wP_r + V \cdot \text{diag} \left( e^{(d-1)\lambda_1 \tau}, e^{(d-1)\lambda_2 \tau}, \ldots, e^{(d-1)\lambda_N \tau} \right) \cdot V^{-1} wP_{2r} + \ldots + V \cdot \text{diag} \left( e^{\lambda_1 \tau}, e^{\lambda_2 \tau}, \ldots, \frac{1}{1 - e^{\lambda_N \tau}} \right) \cdot V^{-1} wP_{d\tau} \quad (10)$$

The subsequent temperature components after $d$ periods ($T_{(d+2)+}, T_{(d+3)+}, \ldots, T_{(d+d)+}$) consist of a similar format but with different linear combinations of the rotation components. We can derive the peak temperature of a rotation by traversing the temperature components $T_{(d+1)+}$ and maxing them. We also readjust the origin by factoring in the linear nature of the matrix transformation.

$$T_{peak} = \max \{ \max \{ B^{-1}T_{amb}G + T_{(d+1)+} \} + \max \{ B^{-1}T_{amb}G + T_{(d+2)+} \} + \ldots + \max \{ B^{-1}T_{amb}G + T_{(d+d)+} \} \} + \max \{ B^{-1}T_{amb}G + T_{(d+d)+} \} \quad (11)$$

V. THREAD ROTATION SCHEDULING

We present a heuristic that provides a thread rotation schedule for S-NUCA many-cores. We call our scheduler HotPotato, and the scheduling it performs HotPotato scheduling. The name takes inspiration from analogous HotSpot routing [23] in computer networks. An S-NUCA many-core comprises topological rings of AMDs, as shown in Figure 3. The cores within the same ring are performance- and thermal-wise homogeneous. The rings become performance-wise constrained and thermal-wise unconstrained as the AMD value increases. HotSpot exploits these concentric rings of AMDs to develop a schedule of synchronously rotating threads. Threads assigned to one ring always rotate within that ring at a given rotational interval. The goal is to develop a schedule that keeps the many-core’s peak temperature $T_{peak}$ lower than the thermal threshold $T_{DTM}$ while maximizing its performance. $T_{DTM}$ is the temperature at which many-core triggers the hardware-controlled Dynamic Thermal Management (DTM) that crashes the many-core’s operating frequency to save it from damage.

Let there be $R$ AMD-based rings on an $n$-core S-NUCA many-core. Let $n_{active}$ be the number of cores required by the $n_{active}$ threads executing with a one-thread-per-core model. The total design space for assigning $n_{active}$ threads to $R$ AMD rings is $\binom{n}{n_{active}}$. We can use Algorithm 1 based on Equation (11) to efficiently determine the peak temperature (thermal safety) of any given schedule (design point) in the design space. Algorithm 1 consists of a design-time phase that pre-calculates the floorplan-based constants (auxiliary matrices $\alpha$ and $\beta$) for instant use at run-time. The algorithm uses the power history of a thread from the last 10 ms in its calculation. However, determining a thermally-safe schedule that also maximizes many-core performance is an NP-hard problem. Therefore, we propose a heuristic for HotPotato to find a near-optimal solution to the problem.

Algorithm 2 describes the greedy heuristic that describes HotPotato decisions when a new thread enters the many-core or when an old thread leaves the many-core. When a new thread enters the many-core, HotPotato tries to assign the thread to the lowest AMD ring for the best performance. Since there is only a
Algorithm 2 HotPotato Scheduling

Input: Floorplan, \( P_{history}, T\_DTM, \text{AMD}, \text{CPI}, \text{Threads} \Gamma \), \( \tau, \Delta, N \)
Output: Response time

1: /*New threads coming*/
2: for each \( AMD_i = AMD_1, AMD_2, \ldots, AMD_t \) do
3: if \( T_{peak} + \Delta < T\_DTM \) then
4: coreLoc ← selectBestCandidate() \( \triangleright T_{peak} \) by Algorithm 1
5: \( T_{peak} \leftarrow \text{updatePeakTemperature}() \) \( \triangleright \text{Update } T_{peak} \)
6: Break
7: else
8: while \( T_{peak} > T\_DTM \) do
9: Sort the threads \( \Gamma \) based on CPI in decreasing order
10: Migrate the thread with lowest CPI to the higher AMD ring
11: \( T_{peak} \leftarrow \text{updatePeakTemperature}() \) \( \triangleright \text{Update } T_{peak} \)
12: while \( T_{peak} > T\_DTM \) do
13: \( \tau \leftarrow \text{updateRotationSpeed}() \) \( \triangleright \text{Update } \tau \)
14: \( T_{peak} \leftarrow \text{updatePeakTemperature}() \) \( \triangleright \text{Update } T_{peak} \)
15: /*Threads finished or thermal headroom > \Delta */
16: while \( T\_DTM - T_{peak} > \Delta \) do
17: for each \( AMD_i = AMD_1, AMD_2, \ldots, AMD_t \) do
18: Sort the threads \( \Gamma \) based on CPI in decreasing order
19: Migrate the threads with the highest CPI to the lower AMD ring
20: \( T_{peak} \leftarrow \text{updatePeakTemperature}() \) \( \triangleright \text{Update } T_{peak} \)
21: if \( T\_DTM - T_{peak} \leq \Delta \) then
22: Break
23: while \( T\_DTM - T_{peak} > \Delta \) do
24: \( \tau \leftarrow \text{updateRotationSpeed}() \) \( \triangleright \text{Update } \tau \)
25: \( T_{peak} \leftarrow \text{updatePeakTemperature}() \) \( \triangleright \text{Update } T_{peak} \)
26: if \( T\_DTM - T_{peak} \leq \Delta \) then
27: Break

There is a possibility of a sudden increase or decrease in thermal headroom (given by the user-defined parameter \( \Delta \)) with a drastic change in power consumption of existing threads on many-core. In such cases, HotPotato adjusts the rotation interval \( \tau \) to deal with the new circumstances.

Complexity Analysis: We discuss the complexity of the design-time phase and run-time phase. In the design-time phase, we calculate the auxiliary matrices \( \alpha \) and \( \beta \). The complexity is \( O(N^2) \). Peak temperature calculation in Algorithm 1 requires iteratively computing the rotation components that take \( O(2.52 N^2) \). In Algorithm 2, in the run-time phase, we assume that the varying rotation speed range is \( \eta \). In the worst case, it traverses \( R \) AMD rings with the complexity \( O(2\eta \ln(\eta) R\delta^3 N^2) \).

VI. EVALUATION

Experimental Setup. We use the interval thermal simulation toolchain HotSniper [12] for simulating an S-NUCA many-core. Table I lists the simulated core and network parameters. We specify The thermal headroom \( \Delta \) at 1°C. We set the idle core power and initial rotation speed at 0.3 W and 0.5 ms, respectively. The ambient and threshold temperatures are set at 45°C and 70°C, respectively.

We use PARSEC [13] benchmark suite to simulate the workload. In particular, we use the streamcluster, x264, bodytrack, canneal, blackscholes, dedup, fluidanimate, and swap-sim benchmarks with sim-small input. We do not use facesim and raytrace benchmarks due to the lack of small-size inputs. We also do not use ferret, freqmine, and vips benchmarks due to unresolved simulation errors in HotSniper.

Baseline. We compare the HotPotato scheduler with the PCMig scheduler [6]. PCMig is the state-of-the-art scheduler for the thermal management of S-NUCA many-cores. It uses DVFS and asynchronous thread migrations as knobs. While HotPotato does not use DVFS, we allow PCMig to perform fine-grained DVFS at a step size of 100 MHz.

Comparative Evaluation with Homogeneous Workload. We fully load the 64-core S-NUCA many-core with varisized multi-threaded instances of the same benchmark. We then simulate a fixed system wherein all instances start execution together. Fig 4(a) reports the normalized makespan of the execution with HotPotato and PCMig schedulers. Results show HotPotato, on average, provides a 10.72% speedup for different benchmarks. Canneal being a memory-intensive benchmark, produces very little heat. Consequently, we observe the lowest speedup gains (0.73%) with Canneal.

Comparative Evaluation with Heterogeneous Workload. We create a random 20-benchmark multi-program multi-threaded workload. We then simulate an open system wherein

<table>
<thead>
<tr>
<th>TABLE I: Core parameters for simulated S-NUCA processor.</th>
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<tbody>
<tr>
<td>Core Parameter</td>
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<tr>
<td>-------------------------------------</td>
</tr>
<tr>
<td>Number of Cores</td>
</tr>
<tr>
<td>Core Model</td>
</tr>
<tr>
<td>L1 cache</td>
</tr>
<tr>
<td>L2 cache</td>
</tr>
<tr>
<td>NoC Latency</td>
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<tr>
<td>Noc link width</td>
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<tr>
<td>The area of core</td>
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</table>
tasks arrive at different arrival rates following a Poisson distribution to create a system under a varying load. HotPotato outperforms PCMig under all load scenarios. The relative speedup gains with HotPotato are minimal when the system is under-loaded or over-loaded, as there is a limited scope of thermal optimizations. In a medium-loaded system, HotPotato provides up to 12.27% improvement over thermal optimizations. In a medium-loaded system, HotPotato provides up to 12.27% improvement over thermal optimizations. In a medium-loaded system, HotPotato provides up to 12.27% improvement over thermal optimizations.

**Run-time Overhead.** Across 10000 runs under full load, HotPotato takes 23.76 μs to calculate a synchronous thread rotation schedule for a 64-core many-core on one of the many-core’s cores. Therefore, HotPotato projects an overhead of 4.75% for a thread rotation epoch of 0.5 ms.

**VII. CONCLUSION & FUTURE WORK**

In this work, we present a scheduler called HotPotato for the thermal management of S-NUCA many-cores. HotPotato builds upon the observation that the performance penalty of thread migration is lower than DVFS on S-NUCA many-cores. It, therefore, uses a heuristic based on synchronous thread migrations rather than commonly employed DVFS and asynchronous thread migrations for managing the thermals of S-NUCA many-cores. The heuristic uses a computationally-efficient method of our design to analytically calculate the peak temperature from thread rotations making HotPotato feasible for run-time use. Thermal interval simulations using the HotSniper toolchain show a thermally-sustainable 10.72% average increase in performance over the state-of-the-art.

**Future Work:** We plan to unify synchronous task rotation with DVFS for even more efficient thermal management of S-NUCA many-cores. Subsequently, we plan to explore the idea of synchronous task rotation with 3D S-NUCA many-cores [24] using the state-of-the-art CoMeT [25] interval thermal simulator designed for 3D-stacked processors.

**REFERENCES**


