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***Abstract*— This article presents the design of a front-end circuit for monolithic active pixel sensors (MAPSs). The circuit operates with a sensor featuring a small, low-capacitance (<2 fF) collection electrode and is integrated into the DPTS chip, a proof-of-principle prototype of 1.5 × 1.5 mm including a matrix of 32 × 32 pixels with a pitch of 15 μm. The chip is implemented in the 65-nm imaging technology from the Tower Partners Semiconductor Company foundry and was developed in the framework of the EP-Research and Development Program at CERN to explore this technology for particle detection. The front-end circuit has an area of 42 μm^2 and can operate with power consumption as low as 12 nW. Measurements on the prototype relevant to the front end will be shown to support its design.**

***Index Terms*— Front-end circuits, low-power circuits, monolithic active pixel sensors (MAPSs).**

I. Introduction

MONOLITHIC active pixel sensors (MAPSs) integrate read-out electronics and sensor in the same silicon die, avoiding the expensive fine-pitch bump bonding of the hybrid pixel sensors, more largely used in the high-energy physics (HEP) experiments. They therefore facilitate significantly the detector assembly and reduce its production cost. The lack of bump bonding helps to obtain higher sensor granularities. With a small pixel area, the sensor capacitance can be made so low to offer, even with a reduced sensor thickness, large Q/C ratios, beneficial for a reduction of the front-end power consumption for a given bandwidth and signal-to-noise ratio (SNR) [1]. The lower material budget of the tracker detectors due to the thinner sensor module and the lighter powering and cooling structures reduces significantly the probability for the particles to be scattered as they emerge from the interaction point. This, together with the lower pixel pitches which tend to give better spatial resolutions, improves the impact parameter and momentum resolution on the reconstructed tracks. MAPSs, therefore, help to satisfy the demand for thin, highly granular, and low-power vertex detectors for future HEP experiments [2], [3], [4].

The inner tracking system (ITS) of the ALICE experiment has recently been upgraded with monolithic sensors in the TowerJazz 180-nm imaging technology [5] and is now taking data. The ALICE collaboration is planning to further upgrade the three innermost layers of the ALICE ITS with wafer-scale monolithic sensors with the size of O(270 × 100 mm) [4]. The target pixel size for this development is O(15 × 15 μm) with a time response within 1 μs. The envisaged power density over the matrix is 20 mWcm^{-2}, as opposed to the 40 mWcm^{-2} of the current ITS, to reduce the amount of material related to the powering and cooling of the detector.

In order to allow higher sensor granularities with complex in-pixel circuitry, the possibility to use for this upgrade and, more generally, for future monolithic sensor developments, a sub-100-nm technology has been explored in the framework of the EP-Research and Development Program at CERN. Finer linewidth technologies also allow a reduction of power consumption with lower supply voltages and offer more integration capabilities with larger reticle and wafer sizes. As significant experience exists in the TowerJazz 180-nm imaging technology, the Tower Partners Semiconductor Company (TPSCo) 65-nm Image Sensor CMOS (ISC) process was considered a possible candidate for these developments. This process is mainly focused on the detection of visible light.

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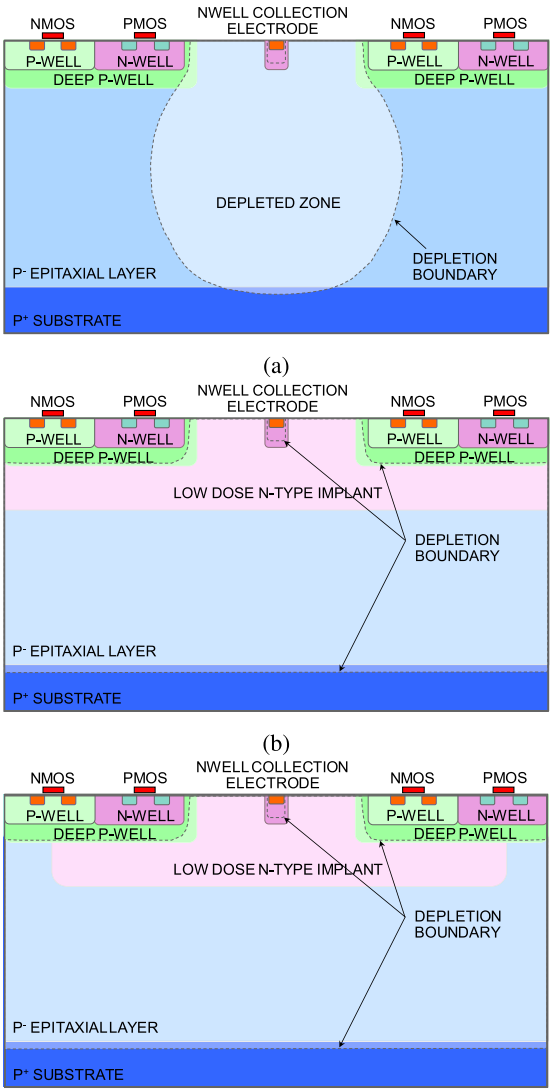

Fig. 1. Cross section of the sensor developed in the TPSCo 65-nm ISC process. (a) Standard process. (b) Modified process with low dose n− implant (c) with a gap in the low dose n− implant (not to scale). From [7].

In order to validate it for HEP applications, a fully-featured monolithic sensor prototype called Digital Pixel Test Structure or DPTS [6] was developed. This article presents the design of the front-end circuit integrated into this structure. Extensive characterization of several aspects of the prototype has been carried out and is still ongoing. The main results relevant to the front end are shown in this article.

II. Sensors

The cross section of the sensor developed in the TPSCo 65-nm ISC technology is shown in Fig. 1 [7]. This sensor features a small collection electrode, the n-well implant in the middle, sitting inside the sensing volume, and a high-resistivity p-type epitaxial layer. The latter is grown on top of a low-resistivity p-type silicon substrate. The in-pixel circuits are placed outside the collection electrode and inside a deep p-well which enables full-CMOS circuitry as it shields the n-wells of the pMOS transistors preventing competition in the charge collection between these n-wells and the collection electrodes. For visible light, the charge is generated within a depth of a few microns. High-energy particles, on the other hand, generate charge over the full thickness of the epitaxial layer which needs to be collected well within the target time response for the event reconstruction. In the case of ionization by a minimum-ionizing particle (MIP), the generated charge is on average ∼60 electron/hole pairs per micrometer traversed [8]. To collect the charge from deep within the epitaxial layer, a reverse bias is applied between the collection electrode and the surrounding p-well and p-type substrate. A depletion volume is thus formed. This starts from the collection electrode and extends within the epitaxial layer with an increasing reverse bias as shown in Fig. 1(a). The carriers generated in the depleted zone are pushed toward the collection electrode by the electric field and are collected by drift. The carriers generated outside the depleted volume move instead by diffusion until they enter the depleted zone and are finally collected by drift. Due to the large areas required by the in-pixel circuitry, it is difficult to obtain depletion of the epitaxial layer over the entire pixel area this way. As done also for the 180-nm technology, the process has been modified to facilitate the depletion of the epitaxial layer and accelerate the charge collection [9]. In the modified process, a uniform ion-implanted low-dose n-layer is added under the deep p-well containing the circuitry and covers the entire matrix/pixel area. The cross section of the sensor with the process modification is shown in Fig. 1(b). In this case, a planar junction is formed deep within the epitaxial layer and the depletion extends immediately over the entire pixel area. The sensor has been additionally modified by creating a gap in the low-dose n− implant along the pixel edges, as shown in Fig. 1(c) [10]. A vertical junction is thus introduced in these regions which enhances the lateral electric field and further accelerates the charge collection. The shorter collection times improve the sensor tolerance to nonionizing energy losses (NIEL) [11]. In fact, they reduce the probability for the carriers to get trapped by the NIEL-induced defects before reaching the collection electrode. With sufficiently low doping of the additional n− implant, the latter is fully depleted in the typical biasing conditions of the sensor. The process modifications, therefore, introduce only a small penalty on the sensor capacitance.

The pixel described in this article has a pitch of 15 μm. The epitaxial layer is 10 μm thick while the gap in the low-dose n− implant along the pixel edges is 2.5 μm. The collection electrode is an octagonal-shaped n-well with a diameter of 1.14 μm and a minimum distance of 1.93 μm from the surrounding p-well of the readout circuitry. Test structures that allow the probing of the analog behavior of the sensor have been submitted in the same run. Measurements on pixels with the same sensor geometry and doping levels show a pixel capacitance <2 fF and subnanosecond collection times [12].

III. Analog Front-End

The implemented front end is a continuously active circuit that performs the reset of the collection electrode, the amplification of the generated charge, and the digitization of the amplified signal through a discrimination stage. In pixel

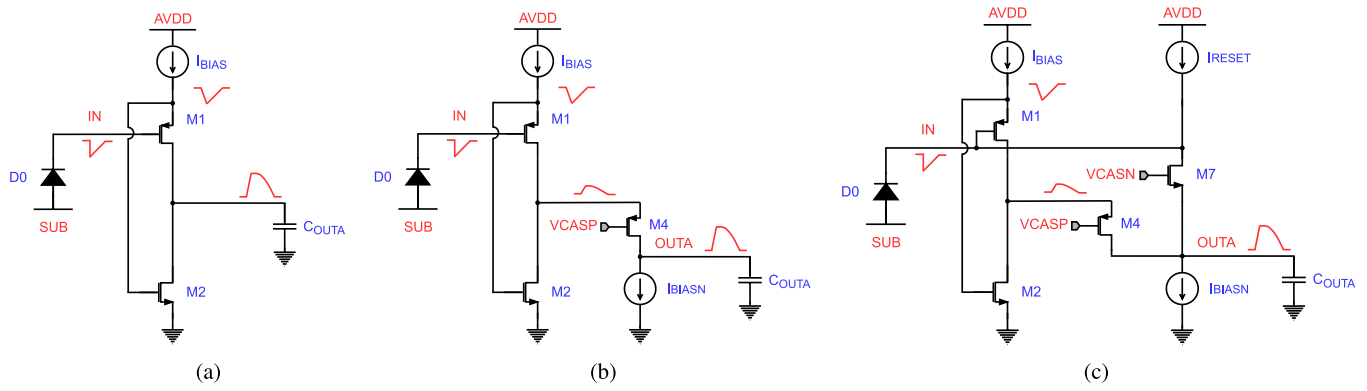

Fig. 2. Front-end schematic: (a) basic principle (b) with cascode (c) with feedback and reset mechanism.

sensors, a charge-sensitive amplifier (CSA) in combination with a discriminator is typically used. The CSA integrates the ionization charge onto a feedback capacitor [13]. In this architecture, for best noise performance, the feedback capacitance should be negligible with respect to one of the sensors [14]. As the latter is in the femtofarad range and much smaller capacitors cannot be easily manufactured, this solution may lead to a noise penalty for the same power consumption. Furthermore, lowering the feedback capacitance to be much smaller than the sensor capacitance will make it also typically smaller than the amplifier output capacitance, degrading the speed of the circuit [15]. To profit from the low sensor capacitance and overcome the aforementioned limitations, the proposed front-end architecture integrates the generated charge into the sensor capacitance itself, as commonly done in image sensors, and the obtained signal is processed, with a novel scheme, by a voltage amplifier, resulting in a more power-efficient solution.

The amplification principle of the front-end is shown in Fig. 2(a). The circuit is directly coupled to the sensor, represented by the diode D0. The input device is the pMOS transistor M1, connected in source-follower configuration with the I_{BIAS} current source, which is the main biasing current of the front end. This transistor is loaded with the nMOS device M2. The gate of the transistor M2 is connected to the source of the input device. Upon a particle crossing, the motion of the generated carriers in the sensor under the effect of the electric field induces a current on the collection electrode [16]. This current is integrated into the sensor capacitance developing a voltage signal with a negative amplitude $\Delta V = Q/C$, where Q is the total generated charge and C is the sensor capacitance. Thanks to the small value of the sensor capacitance, already the charge released by a MIP generates a voltage signal of tens of mV. A replica of this signal is then obtained on the source of the input transistor due to its source-follower action and so on the gate of the transistor M2. The latter behaves as a common-source device and a voltage signal is thus obtained on the drains of the two transistors. This circuit was inspired by the front end used in the monolithic sensor installed in the current ALICE ITS [17]. This front-end topology was also adapted in [18] for a 25 ns time response as required by other experiments at the HL-LHC. In this circuit, the connection between the source of the input follower to the corresponding amplifying device is done via a capacitor. To achieve large gains, this capacitor needs to be large, occupying a significant fraction of the entire circuit area. The circuit has therefore been modified to remove this element and obtain a more compact solution. For good performance, the small sensor capacitance has to be preserved. Its value is not only determined by the sensor junction as contributions also come from the input line and the gate of the input transistor. After settling, the source-follower action of the input transistor reduces the contribution of its gate–source capacitance to the effective sensor capacitance. To further reduce the front-end input capacitance, a cascode is used to move the high-impedance output node from the drain of the input transistor over another branch, as shown in Fig. 2(b). In this circuit, as the drain of the input transistor exhibits a lower impedance and hence a lower gain, the Miller effect on its gate–drain capacitance is reduced and so is its contribution to the sensor capacitance. The I_{BIASN} current source introduced to bias the cascode draws nominally 1/10 of the I_{BIAS} current from the main branch. The output node therefore features a higher impedance compared to the previous scheme and larger gains are also achieved. In these circuits, both the current in the input transistor and the potential on its source are defined. The dc voltage on the input node must therefore be set very precisely for the input transistor to conduct the I_{BIAS} current and operate in saturation. A more practical implementation of the circuit is shown in Fig. 2(c). In this scheme, an input–output feedback that adjusts the input voltage has been introduced. This feedback also resets the front end after a particle hit and compensates for the sensor leakage. A small fraction of the I_{RESET} current is indeed taken by the sensor leakage current. The remaining current flows in the transistor M7 which is the feedback element connected across the input and output nodes. Upon a hit, as the voltage on the collection electrode drops and the output voltage rises, the gate–source voltage of the transistor M7 reduces, forcing more current from the I_{RESET} current source into the collection electrode which charges it back to its original value. The I_{RESET} current is typically orders of magnitude lower than the main I_{BIAS} current. A low value for this current is necessary to implement sufficiently low-frequency feedback and avoid clipping the high-frequency input signals.

The complete front-end circuit which includes the amplifier and discriminator is shown in Fig. 3. In the amplification stage,

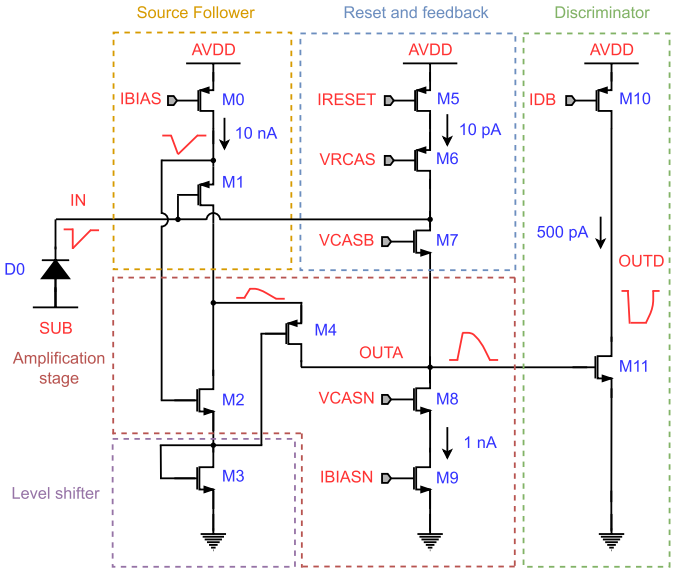

Fig. 3. Complete front-end schematic with discriminator.

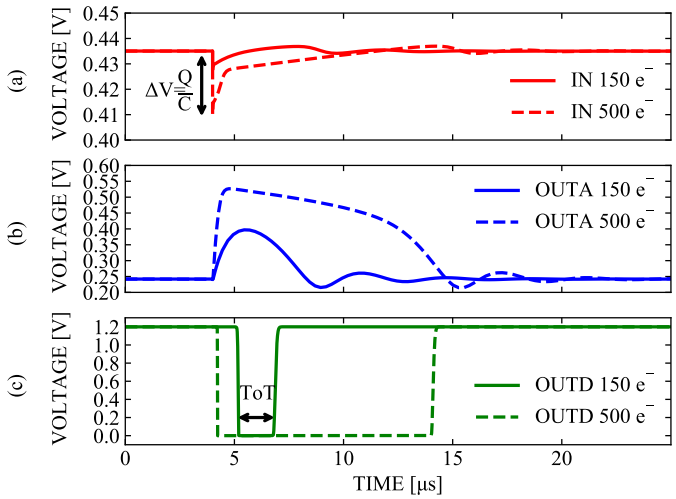

Fig. 4. Front-end simulated transient response with a threshold of 140 e⁻ for an injected charge of 150 e⁻ (solid lines) and 500 e⁻ (dashed lines): (a) signals on the collection electrode, (b) signals at the output of the amplifier, and (c) signals at the output of the discriminator.

a diode-connected nMOS transistor has been inserted between the source of the transistor M2 and the ground to shift up its source voltage. With this modification, part of the buffered signal on the source of the input transistor drops across the diode-connected device reducing the signal available to the amplifying device M2 and therefore the front-end gain. This modification is however necessary to obtain sufficient margins for the input transistor in all the operating conditions. The input transistor is placed, together with the transistor M4, in a separated n-well connected to its source to eliminate the body effect and achieve a gain closer to unity for the input follower. The I_{BIASN} current source, implemented by the transistor M9, is cascoded to increase the output impedance and therefore the gain. The I_{RESET} current source, implemented by the transistor M5, is also cascoded to reduce the systematic variations on this current. The cascode transistor M6, as well as the feedback transistor M7, is designed with a minimum width to minimize as much as possible the capacitive load on the sensor. The discrimination is performed by a common-source stage, the transistors M10 and M11, which can be better seen in this case as a current comparator. In a steady state, the current in the transistor M11 is defined by the output baseline of the amplifier. The transistor M10 is biased to provide an I_{DB} current larger than the standby current in M11, charging the node OUTD to the supply voltage. As the amplifier output signal rises upon a particle hit, the current in the transistor M11 increases, eventually exceeding the I_{DB} current and discharging the output node to the ground. The charge threshold is therefore defined by the combination of the amplifier gain, its output baseline (through the V_{CASB} and I_{RESET} biases), and the discriminator I_{DB} current setting.

The front end was designed to be within the specifications of the ALICE ITS upgrade and dissipate, for the target pitch of 15 μm, a power density of $\sim$5 mWcm^{-2} while featuring sub-μs reaction times. The circuit is therefore to be optimized for timing performance given this power budget. The bandwidth of the input follower is mainly related to the transconductance g_m of the input transistor and its load capacitance, dominated by the gate capacitance of the device M2. The gain-bandwidth product of the amplification provided by the transistor M2 is defined by its transconductance g_m and the output capacitance C_{OUTA}. Essentially, the peaking time of the output waveform decreases with a higher transconductance g_m of the amplifying devices and a lower output capacitance C_{OUTA}. The transistors' dimensions and the layout are therefore optimized with postlayout simulations for a large transconductance g_m of the amplifying devices and a low output capacitance C_{OUTA}, which is $\lesssim$5 fF. To satisfy the power requirement, the main biasing current I_{BIAS} needs to be within 10 nA. The I_{BIASN} current is set ten times lower than I_{BIAS} and so to 1 nA. The I_{RESET} current is instead set to 10 pA, small enough to avoid filtering the input signals within the bandwidth of the amplifier with these currents. The quiescent current in the discriminator can be set as low as hundreds of picoamper thanks to the large gain provided by the amplification stage. With a supply voltage of 1.2 V, the total power consumption of the front-end is $\sim$12 nW at these bias settings. Although the circuit is optimized for low-power consumption, all its parameters can be varied across a wide range of values. In particular, to enhance the front-end speed, its power consumption can be increased by raising the I_{BIAS} and I_{BIASN} currents maintaining a 10:1 ratio as done in the measurements below.

A parasitic-extracted simulation of the front-end with a charge threshold set to $\sim$140 e$^-$ is shown in Fig. 4. The solid lines show the response for an input charge of 150 e$^-$, whereas the dashed lines for a charge of 500 e$^-$. In the simulation, the sensor is modeled as a capacitance of 1 fF in parallel with a leakage current source of 10 fA. The charge is injected with a rectangular current pulse on the sensor, i.e., uniformly over 100 ps. The red curves represent the input signals and show that the voltage step on the collection electrode is proportional to the injected charge. The blue curves represent instead the amplified signals on OUTA. The

front-end gain is inherently nonlinear: as the voltage on OUTA rises, the transistor M7 dynamically turns off, offering a larger impedance on the output node, and the gain increases. Indeed, for a charge of a few electrons, the gain is ∼0.7 mV/e$^-$, whereas it is ∼1 mV/e$^-$ with an injected charge of 150 e$^-$, i.e., around threshold, as shown in Fig. 4. For larger charges, the analog output signal on OUTA dynamically pushes the cascode transistor M4 out of the saturation region which makes it ineffective and the front-end gain therefore starts to drop. For an injected charge of 500 e$^-$ as in the simulation, the front-end gain is ∼0.57 mV/e$^-$. Conversely, the Time-over-Threshold (ToT) of the analog output signals, i.e., the duration of the discriminator output pulses shown in green in Fig. 4, has a linear dependence on the input charge in a wide range of values. The ToT is indeed related to the time needed for the collection electrode to be reset to its steady-state value after a particle hit. As the input charge is large enough for the analog output signal to completely shut off the feedback device M7, the I_{RESET} current entirely flows into the collection electrode which is therefore charged back up linearly with a constant current.

To operate the sensor reliably with a low noise hit rate, the charge threshold has to be sufficiently larger than the front-end equivalent noise charge (ENC) and pixel-to-pixel threshold variation due to mismatch. A low noise and high pixel-to-pixel uniformity have to be therefore ensured to be able to set sufficiently low charge thresholds to determine particle hits and obtain high detection efficiencies. Apart from the main amplifying devices which have a large transfer function to the output node, a relevant noise contributor is the transistor M5 which provides the I_{RESET} current. This current is directly connected to the collection electrode and contributes to the input parallel noise. For this reason, a sufficiently low value of said current has to be ensured to prevent it from excessively increasing the input noise. On the other hand, this current has to be higher than the sensor leakage for the feedback network to be able to perform the leakage current compensation. The transistor M5 providing the I_{RESET} current represents also one of the most critical devices for the pixel-to-pixel threshold variation. In fact, the I_{RESET} current defines the transconductance g_m of the feedback device M7 and has a large impact on the feedback speed and amplifier gain. For this reason, it is designed with a low aspect ratio and a large area, representing one of the largest components of the circuit. Another relevant contributor to the pixel-to-pixel threshold variation in the amplification stage is the transistor M7. The gate–source voltage of this transistor, in combination with the I_{RESET} current, defines the amplifier output baseline and thus the standby current in the discriminator and its switching threshold. As it loads the output node, this transistor has to be narrow to prevent increasing the output capacitance. The main critical device in the discriminator stage is the input transistor M11. A variation of its threshold voltage, indeed, directly shifts the switching point of the discriminator, resulting basically in an input offset. Similar to the transistor M7, this device has to be kept small for a small output capacitance. The size of these transistors, therefore, results from a compromise between gain, speed, and threshold dispersion. In order to estimate

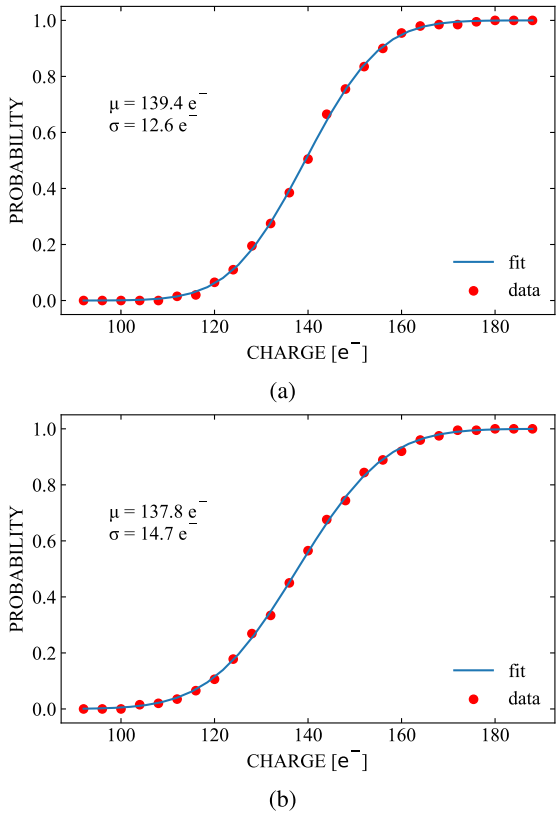

Fig. 5. Simulated hit probability as a function of the injected charge with (a) transistors' mismatch and (b) nominal transistors but added transient noise. 200 runs per data point.

the pixel-to-pixel threshold variation and the ENC, Monte Carlo and transient-noise simulations have been performed to evaluate the front-end probability of generating a hit as a function of the injected charge, obtaining the curves shown in Fig. 5. For each injected charge, 200 runs have been performed. These simulations have been performed with an I_{RESET} current of 10 pA, high enough to operate the chip even after some level of irradiation. The mean value of the Gaussian error fit to the curves gives the front-end nominal threshold, which is ∼140 e$^-$, whereas its standard deviation gives the pixel-to-pixel threshold variation and the ENC in the case of the Monte Carlo [Fig. 5(a)] and transient-noise simulations [Fig. 5(b)], respectively, which are ∼12.6 and ∼14.7 e$^-$.

The layout of the pixel is shown in Fig. 6. The 1.14 μm octagonal-shaped collection electrode with a minimum distance of 1.93 μm from the p-well containing the circuitry is placed in the center. The voltage on the collection electrode is adjusted by the negative input–output feedback of the front end, typically to a few hundred millivolts. To increase the sensor reverse bias, therefore, a net separate from the circuitry ground is dedicated to the deep p-well containing the circuits and to the p-type substrate, which can be biased down to −6 V. The front end is placed below the collection electrode in the layout view of Fig. 6 and occupies, together with a decoupling capacitor of 20 fF, an area of ∼42 μm^2. A testing circuit that allows to capacitively inject a tuneable charge into the collection electrode is also integrated into the pixel. It is placed above the collection electrode in the layout view

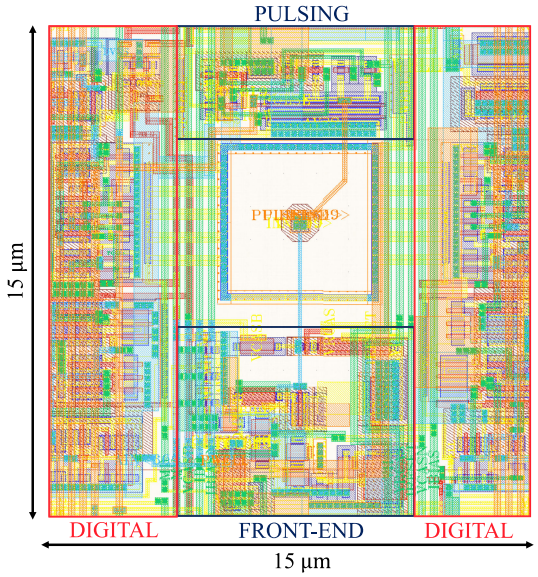

Fig. 6. Layout of the pixel.

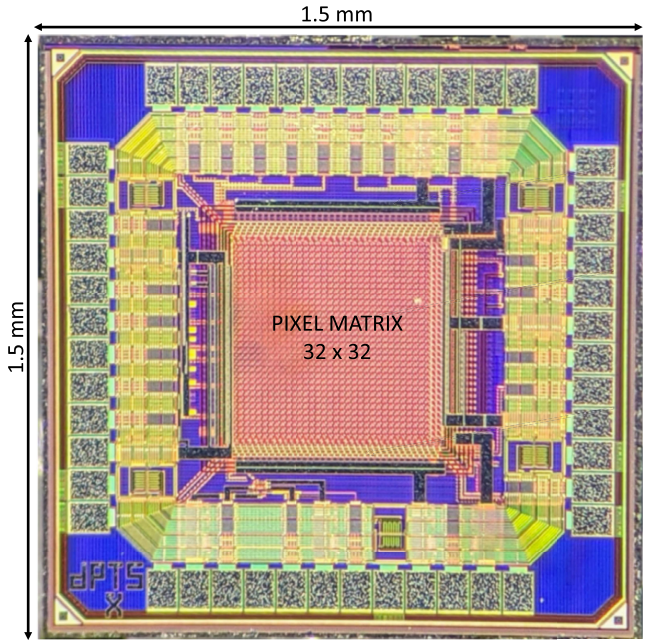

Fig. 7. Picture of the prototype DPTS chip.

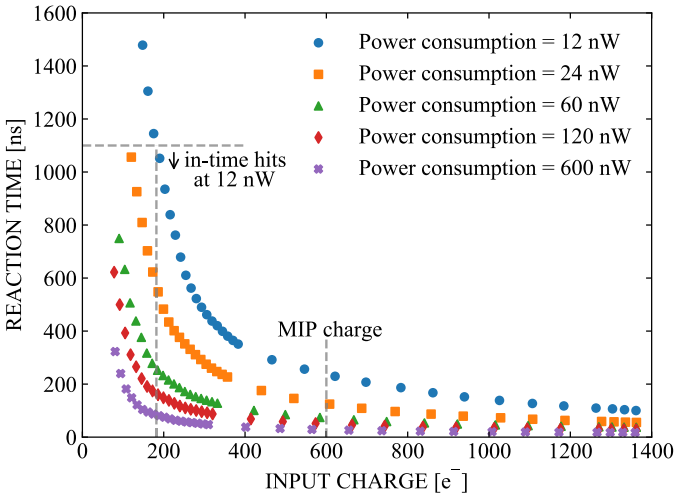

Fig. 8. Measured front-end time walk curve.

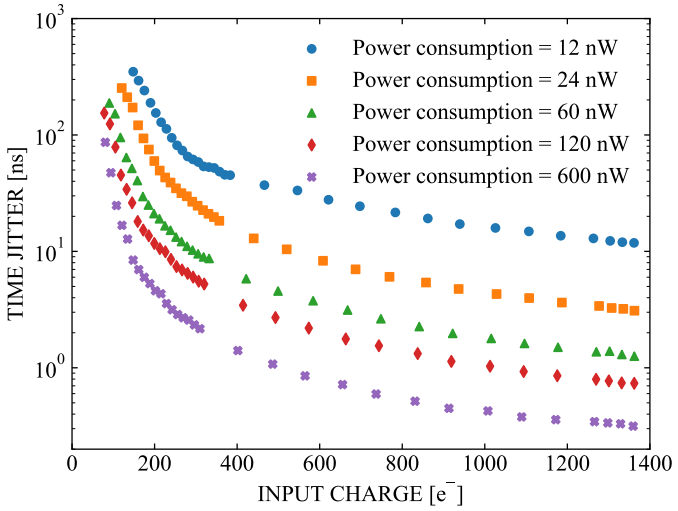

Fig. 9. Measured front-end time jitter.

and requires an area of ∼17 μm^2. The rest of the pixel is occupied by the digital readout circuits, for a total pixel area of 15 × 15 μm. With this pitch, the analog power density over the matrix is ∼5.3 mWcm^{-2}, within the requirements of the ALICE ITS upgrade. The digital readout features an asynchronous event-driven logic [19]. It generates a stream of pulses that encode the coordinates of the hit pixels and the ToT information. These pulses are transmitted to the periphery immediately upon a hit on a single-bit bus which reads out the entire matrix. This signal is then sent OFF-chip via a differential CML driver. The DPTS prototype has a size of 1.5 × 1.5 mm and integrates a matrix of 32 × 32 pixels. A serial interface allows one to communicate with the chip and write in a triplicated shift register. The latter is responsible for configuring the chip and allows it to mask off each pixel in case it generates an excessive noise hit rate or selects it for charge injection. The injection is then triggered externally by sending a pulse on a specific interface pad. The biases of the analog circuitry are provided by peripheral biasing structures and are tuned externally via dedicated interface pads. A picture of the DPTS chip under a microscope is shown in Fig. 7.

IV. Front-End Characterization

Tests on the front end have been performed with a custom system that supplies biases and control signals to the chip and records its differential CML output on an oscilloscope. Laboratory measurements mainly involved charge injections through the in-pixel pulsing circuitry. The injection capacitance has been calibrated by comparing the ToT of signals obtained with charge injections and exposure to an ^{55}Fe source. The front-end speed has been tested with the time walk curve, i.e., the time for the amplifier output to reach the discriminator threshold as a function of the input charge. This curve has been evaluated for different settings of the circuit where a faster reaction is obtained by increasing the power consumption from

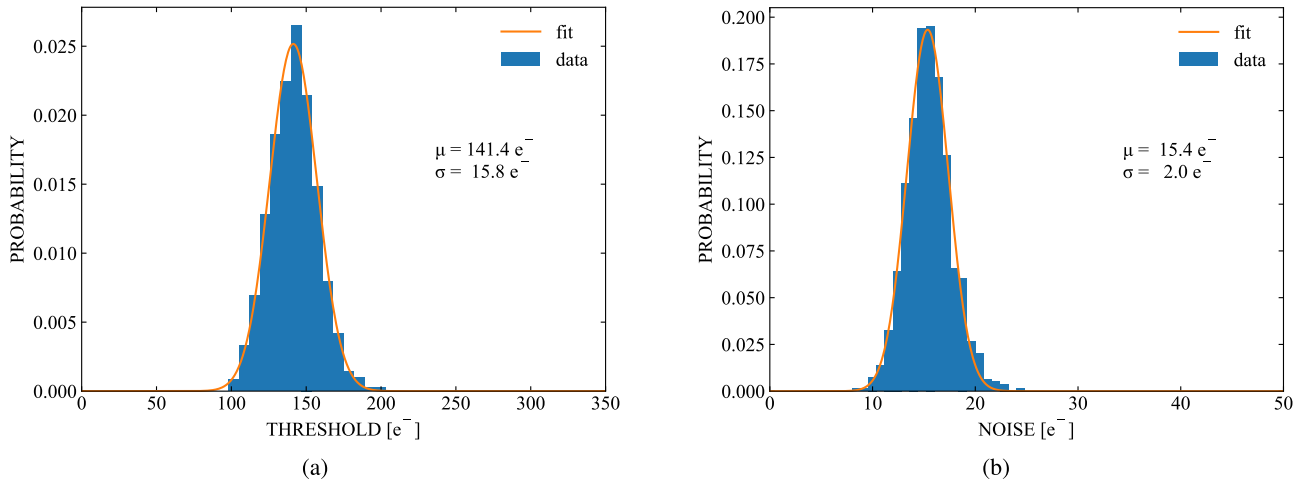

Fig. 10. Distribution of (a) threshold and (b) ENC with a power consumption of 12 nW and an I_{RESET} current of 10 pA.

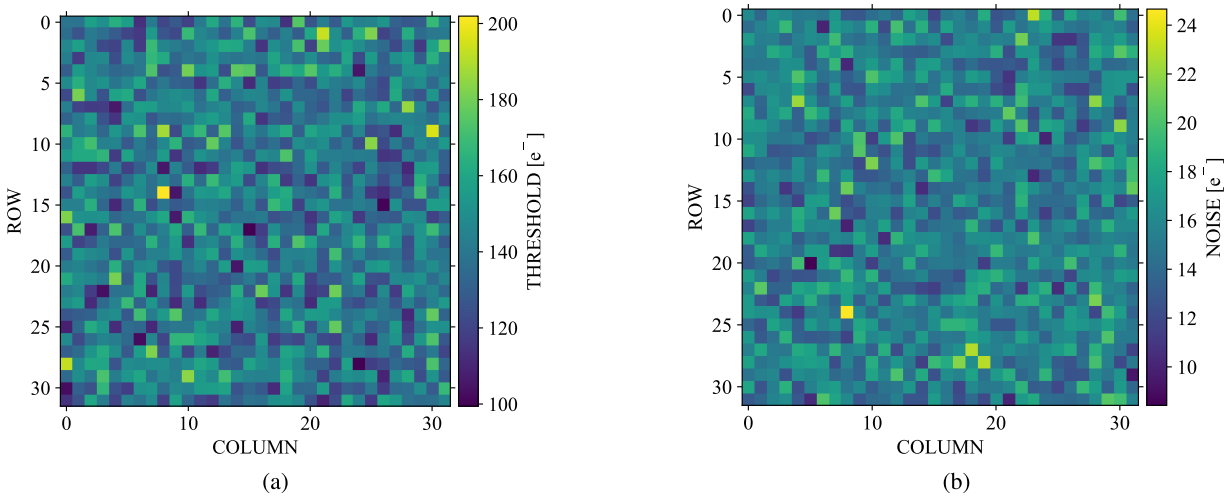

Fig. 11. Two-dimensional map of (a) threshold and (b) ENC with a power consumption of 12 nW and an I_{RESET} current of 10 pA.

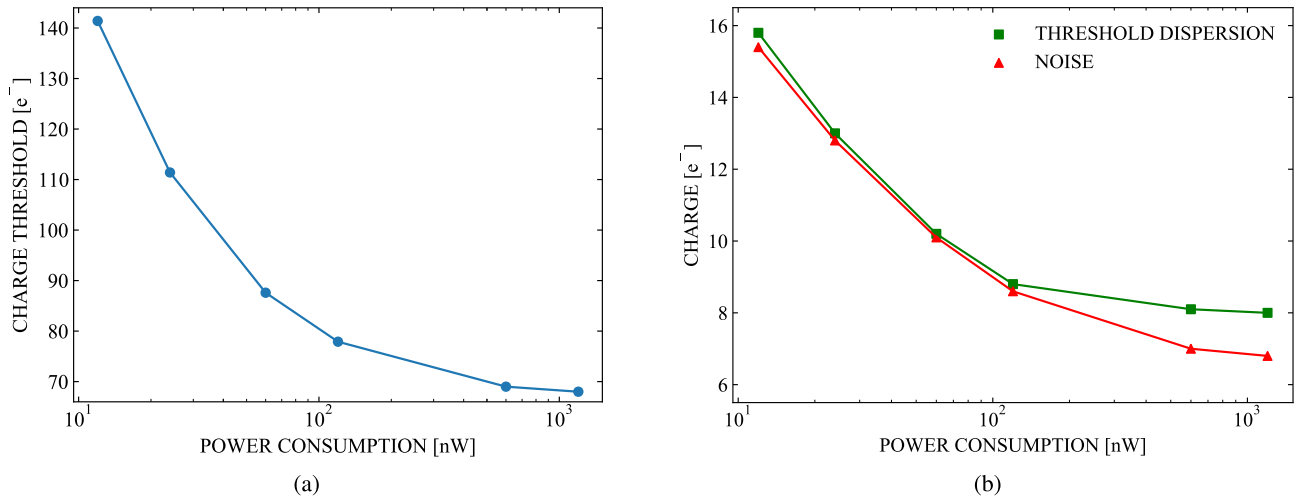

Fig. 12. Trend of (a) nominal threshold and (b) threshold dispersion and noise versus power consumption.

12 nW up to 600 nW. The obtained results are shown in Fig. 8. The measurements have been performed using as a time reference the charge injection trigger pulse sent to the chip. In order to do so, this signal is sent to the readout oscilloscope together with the chip CML output. The difference between the time of arrival of these two signals provides the delay of

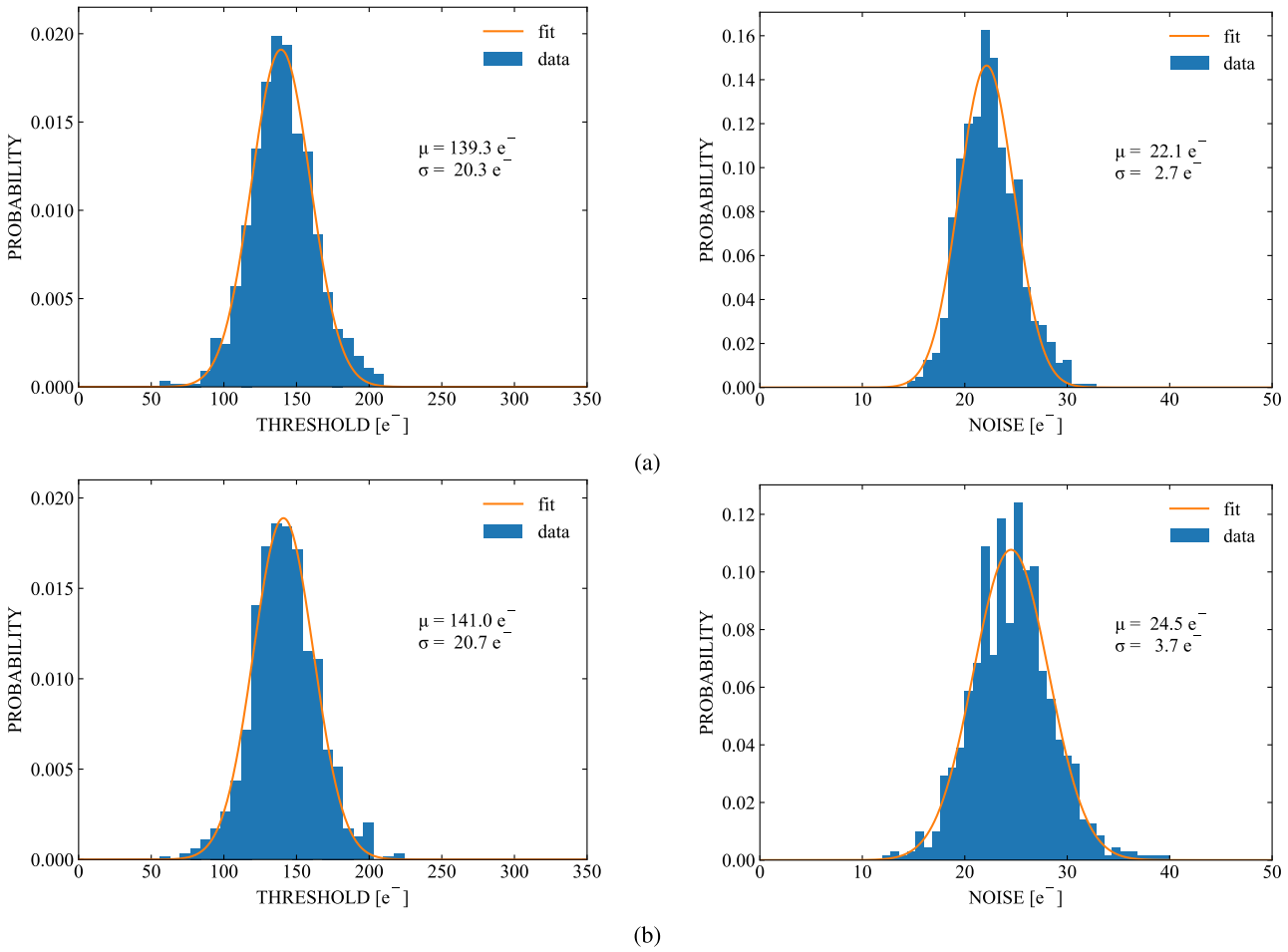

Fig. 13. Distributions of threshold and ENC with a power consumption of 12 nW and an I_{RESET} current of 35 pA for (a) unirradiated sample and (b) sample irradiated at 10^{15} 1 MeV $n_{\mathrm{eq}}/\mathrm{cm}^2$ and 1 Mrad.

the entire readout chain which is however largely dominated by the contribution of the front-end amplifier. The plotted values are the average of the results obtained by pulsing each pixel 25 times. The rms of these values are instead plotted in logarithmic scale in Fig. 9 and provide the corresponding front-end time jitter. As can be noticed from Fig. 8, in the lowest power mode, hits with charges $\gtrsim$1200 e$^-$ have a delay close to the minimum value of ∼100 ns. For the ALICE experiment, an event is in time if it arrives within 1 μs from the lowest possible delay. In-time events are obtained for input charges $\gtrsim$200 e$^-$, which is ∼35% of the charge released by a MIP in the epitaxial layer of the sensor. For this input charge, the front-end time jitter is ∼150 ns and reduces down to ∼10 ns for high input charges ($\gtrsim$1200 e$^-$). If a time response within 25 ns is required, as in other experiments at the HL-LHC, this can be obtained for charges $\gtrsim$350 e$^-$ by increasing the power consumption to 600 nW. The larger power consumption also reduces the front-end time jitter which spans from a few nanoseconds at the in-time threshold charge, down to 0.3 ns for high input charges ($\gtrsim$1200 e$^-$).

Charge test injections allow also to evaluate figures as threshold and noise: varying the charge injected into a pixel, an s-curve as the one in Fig. 5(b) can be obtained and the front-end threshold and noise extracted through the Gaussian error fit as done before. The threshold and noise distributions of an entire matrix operating the front end with a power consumption of 12 nW are shown in Fig. 10. The average threshold is ∼140 e$^-$ with a standard deviation of ∼15.8 e$^-$. The noise distribution has an average of ∼15.4 e$^-$. These values match fairly well the simulated ones shown in Fig. 5. Bidimensional maps of the threshold and noise of each pixel are reported in Fig. 11 and these show random patterns indicating the absence of systematic effects over the matrix. As for the timing measurements, the same procedure has been repeated with larger power consumptions, and the results are summarized in Fig. 12. In particular, the plot in Fig. 12(a) reports the nominal threshold as a function of the power consumption which shows a decreasing trend. As the configuration of the discriminator is unvaried in the different settings, this indicates a larger amplifier gain which, in combination with the higher currents, leads to a lower threshold dispersion and noise, shown in Fig. 12(b). During these measurements also the fake-hit rate (FHR) has been monitored. It is defined as the number of hits per pixel and second in the absence of external stimuli and is evaluated as the number of hits in randomly triggered oscilloscope acquisitions divided by their duration and the total number of pixels. No pixel-by-pixel tuning of the threshold is possible with this

TABLE I
FRONT-END SPECIFICATIONS WITH A THRESHOLD OF 140 e^-

Parameter		Value
Area		42 μm^2
Power consumption		12 nW
In-time threshold (for a 1 µs time window)		200 e^-
Time jitter	at the in-time threshold	150 ns
	for high charges ($\gtrsim$ 1200 e^-)	10 ns
Threshold dispersion	unirradiated with I_{RESET} = 10 pA	15.8 e^-
	unirradiated with I_{RESET} = 35 pA	20.3 e^-
	10^{15} 1 MeV n_{eq}/cm^2 and 1 Mrad with I_{RESET} = 35 pA	20.7 e^-
ENC	unirradiated with I_{RESET} = 10 pA	15.4 e^-
	unirradiated with I_{RESET} = 35 pA	22.1 e^-
	10^{15} 1 MeV n_{eq}/cm^2 and 1 Mrad with I_{RESET} = 35 pA	24.5 e^-

prototype. In all the configurations, the FHR stays below a value of 10^{-2} pixel^{-1}s^{-1} with a minimal amount of masked pixels (<5).

A number of DPTS samples have been irradiated with neutrons at the TRIGA reactor in Ljubljana [20]. During irradiation, the chips were not powered. After irradiation, the chips are stored at low temperatures (below −20 °C) to avoid annealing of the radiation damage. The measurements on these samples are however performed at room temperature. Charge injection tests have been performed on samples irradiated up to a NIEL fluence of 10^{15} 1 MeV n_{eq}/cm^2 and a TID of 1 Mrad due to background radiation. The chip still shows complete functionality and even full efficiency ($\gtrsim$99%) at room temperature after these levels of irradiation [6]. However, a larger I_{RESET} current has to be set for the reset network to be able to perform the compensation of the sensor leakage current, which increased from less than 1 to ∼10 pA due to the irradiation. For a fair comparison, tests on unirradiated samples have been repeated with the larger I_{RESET} current, which is 35 pA. The distributions of threshold and ENC for an unirradiated sample and a sample irradiated at 10^{15} 1 MeV n_{eq}/cm^2 and 1 Mrad with a front-end power consumption of 12 nW are shown in Fig. 13. The discriminator settings have been adjusted to obtain a similar threshold in both cases. The ENC of the unirradiated sample is 22.1 e^-, larger than the value shown in Fig. 10 due to the larger I_{RESET} current, and increases to 24.5 e^- for the sample irradiated at 10^{15} 1 MeV n_{eq}/cm^2 and 1 Mrad. The threshold dispersion is instead 20.3 e^- for the unirradiated sample and marginally higher for the irradiated one at 20.7 e^-.

V. CONCLUSION

This article described the design and characterization of a front-end for MAPSs. The circuit is implemented in the TPSCo 65-nm ISC technology and integrated into the DPTS chip, a prototype developed in the framework of the EP-Research and Development Program at CERN to validate this technology for HEP applications. The sensor features a small collection electrode with a diameter of 1.14 μm to achieve a low capacitance (<2 fF), key for low-power operation for a given ENC and bandwidth. The circuit was designed to comply with the specifications of the ALICE ITS upgrade. Furthermore, it is optimized for low noise and pixel-to-pixel variation to achieve low thresholds. DPTS samples have been extensively characterized before and after irradiation to evaluate the front-end performance. The main figures are summarized in Table I. The circuit shows promising results and further studies will be carried out toward the ALICE ITS upgrade.

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REFERENCES

[1] W. Snoeys, "Monolithic pixel detectors for high energy physics," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 731, pp. 125–130, Dec. 2013, doi: 10.1016/j.nima.2013.05.073.

[2] *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, document CERN-LHCC-2017-021, ATLAS-TDR-030, ATLAS Collaboration, Geneva, Switzerland, 2017. [Online]. Available: https://cds.cern.ch/record/2285585

[3] *The Phase-2 Upgrade of the CMS Tracker*, document CERN-LHCC-2017-009, CMS-TDR-014, CMS Collaboration, Cessy, France, 2017. [Online]. Available: https://cds.cern.ch/record/2272264

[4] L. Musa and W. Riegler, *Letter of Intent for an ALICE ITS Upgrade in LS3*, document CERN-LHCC-2019-018, LHCC-I-034, 2019. [Online]. Available: https://cds.cern.ch/record/2703140

[5] M. Mager, "ALPIDE, the monolithic active pixel sensor for the ALICE ITS upgrade," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 824, pp. 434–438, Jul. 2016, doi: 10.1016/j.nima.2015.09.057.

[6] G. A. Rinella et al., "Digital pixel test structures implemented in a 65 nm CMOS process," 2022, *arXiv:2212.08621*.

[7] W. Snoeys et al., "Optimization of a 65 nm CMOS imaging process for monolithic CMOS sensors for high energy physics," *Proc. Sci.*, vol. 420, p. 83, Mar. 2023, doi: 10.22323/1.420.0083.

[8] S. Meroli, D. Passeri, and L. Servoli, "Energy loss measurement for charged particles in very thin silicon layers," *J. Instrum.*, vol. 6, no. 6, Jun. 2011, Art. no. P06013, doi: 10.1088/1748-0221/6/06/p06013.

[9] W. Snoeys et al., "A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 871, pp. 90–96, Nov. 2017, doi: 10.1016/j.nima.2017.07.046.

[10] M. Munker et al., "Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance," *J. Instrum.*, vol. 14, no. 5, May 2019, Art. no. C05013, doi: 10.1088/1748-0221/14/05/c05013.

[11] M. Dyndal et al., "Mini-MALTA: Radiation hard pixel designs for small-electrode monolithic CMOS sensors for the High Luminosity LHC," *J. Instrum.*, vol. 15, no. 2, Feb. 2020, Art. no. P02005, doi: 10.1088/1748-0221/15/02/p02005.

[12] W. Deng et al., "Design of an analog monolithic pixel sensor prototype in TPSCo 65 nm CMOS imaging technology," *J. Instrum.*, vol. 18, no. 1, Jan. 2023, Art. no. C01065, doi: 10.1088/1748-0221/18/01/C01065.

[13] F. Krummenacher, "Pixel detectors with local intelligence: An IC designer point of view," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 305, no. 3, pp. 527–532, Aug. 1991, doi: https://doi.org/10.1016/0168-9002(91)90152-G.

[14] E. Gatti and P. F. Manfredi, "Processing the signals from solid-state detectors in elementary-particle physics," *La Rivista del Nuovo Cimento*, vol. 9, no. 1, pp. 1–146, Jan. 1986, doi: 10.1007/BF02822156.

[15] A. Rivetti, *CMOS: Front-End Electronics for Radiation Sensors*. Boca Raton, FL, USA: CRC Press, 2017, p. 263.

[16] S. Ramo, "Currents induced by electron motion," *Proc. IRE*, vol. 27, no. 9, pp. 584–585, Sep. 1939, doi: 10.1109/JRPROC.1939.228757.

[17] D. Kim et al., "Front end optimization for the monolithic active pixel sensor of the ALICE Inner Tracking System upgrade," *J. Instrum.*, vol. 11, no. 2, Feb. 2016, Art. no. C02042, doi: 10.1088/1748-0221/11/02/C02042.

[18] F. Piro et al., "A 1-μW radiation-hard front-end in a 0.18-μm CMOS process for the MALTA2 monolithic sensor," *IEEE Trans. Nucl. Sci.*, vol. 69, no. 6, pp. 1299–1309, Jun. 2022, doi: 10.1109/TNS.2022.3170729.

[19] L. Cecconi et al., "Design and readout architecture of a monolithic binary active pixel sensor in TPSCo 65 nm CMOS imaging technology," *J. Instrum.*, vol. 18, no. 2, Feb. 2023, Art. no. C02025, doi: 10.1088/1748-0221/18/02/C02025.

[20] L. Snoj, G. Žerovnik, and A. Trkov, "Computational analysis of irradiation facilities at the JSI TRIGA reactor," *Appl. Radiat. Isot.*, vol. 70, no. 3, pp. 483–488, Mar. 2012, doi: 10.1016/j.apradiso.2011.11.042.