On the cutting edge of semiconductor sensors: towards intelligent X-ray detectors

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Semiconductor sensors

Semiconductors are eminently suitable as conversion material for particle and radiation detectors because of their conductivity, which is between that of conductors and insulators. To understand what determines conductivity, the quantum mechanical behaviour of electrons in atomic lattices must be considered.
The first section of this chapter discusses the principles of semiconductor physics [20–24] and signal formation. Section 2.2 describes the basic building blocks of semiconductor sensors: the p-n junction and metal-semiconductor contacts. Section 2.3 goes into detail on sensor fabrication, with a specific focus on wafer dicing techniques, since the sensor's performance at the edge is largely determined by the method used. The last section covers sensor design in terms of different electrode topologies, particularly focussing on edgeless sensors.

2.1 Physics concepts

2.1.1 Band theory

According to quantum mechanics [25, 26] each particle occupies a quantum state, which is described by a wave function. The square modulus of this wave function represents the probability density of measuring this particle at a given position and time. If a particle is bound to a potential, for example an electron that is bound to a nucleus, it can only occupy states of discrete energy. As a consequence, electrons are located at discrete distances from the nucleus.
Now, what happens when the spacing between atoms decreases to the order of the atomic radius? Electrons occupying the same quantum state will approach each other and their probability density functions will start to overlap. According to Pauli's exclusion principle [27], however, no two electrons can occupy the same quantum state simultaneously. As a result, the energy levels split up. It can be thought of as if one of the levels is pushed slightly upwards, the other slightly downwards. The new wave functions are a linear combination of the two individual wave functions. When many atoms are brought together, as is the case in an atomic lattice, the energy states will be divided into numerous levels.

These levels are so close to each other that they almost form a continuum. They can be seen as a band of energy states.
In this way, crystals have bands of allowed and forbidden states. The distribution of electrons over the allowed states is described by the Fermi-Dirac function [28]:

$$f_{\mathrm{F}}(E) = \frac{1}{1 + e^{\left(\frac{E - E_{\mathrm{F}}}{kT}\right)}} . \tag{2.1}$$

This function gives the probability that a state is occupied by an electron. E is the energy of the quantum state, E_{F} is the energy of the Fermi level[1], k is Boltzmann's constant and T the absolute temperature. The Fermi level is defined as the highest energy level occupied at absolute zero. In other words, all states of the energy band directly below the Fermi level are filled by electrons at 0 K. These electrons close the outer valence shells and are responsible for the bonding between atoms. This energy band is known as the valence band. The band immediately above the Fermi level is completely empty at 0 K, but can be filled with electrons from the valence band when the temperature increases or when excited by a photon or charged particle. These liberated electrons can freely migrate through the crystal and do not contribute to the bonding anymore. They are responsible for conduction. Hence, this band is called the conduction band. For both semiconductors and insulators there exists a forbidden area between the valence and conduction band: the band gap. No states exist in this area. The width of the band gap is determined by the energy difference E_g between the highest level in the valence band and the lowest in the conduction band and depends on the interatomic spacing. It fundamentally determines the ease with which valence electrons can surmount the band gap and serve as conduction electrons. Figure 2.1 is a schematic representation of the upper edge of the valence band relative to the lower edge of the conduction band for conductors, semiconductors and insulators. Conductors have no band gap; their valence and conduction bands overlap. Insulators have a band gap of 5 eV or greater. In the case of semiconductors, the width of the forbidden zone is of the order of 1 eV. Therefore, only little energy is needed to bring electrons into the conduction band. When this transition occurs, the electrons leave behind empty states in the valence band, called holes [29]. A valence electron can fill such an empty state, leaving behind another hole. Holes can therefore migrate and also contribute to conduction. However, they cannot be considered free carriers, since they are part of the crystal.

2.1.2 Carrier concentration

The conductivity of a semiconductor is proportional to the concentration of free carriers. This concentration is dependent on the position of the Fermi level relative to the band edges. In the Boltzmann approximation [30], the electron concentration n and hole

[1] E_{F} is also referred to as the Fermi energy.

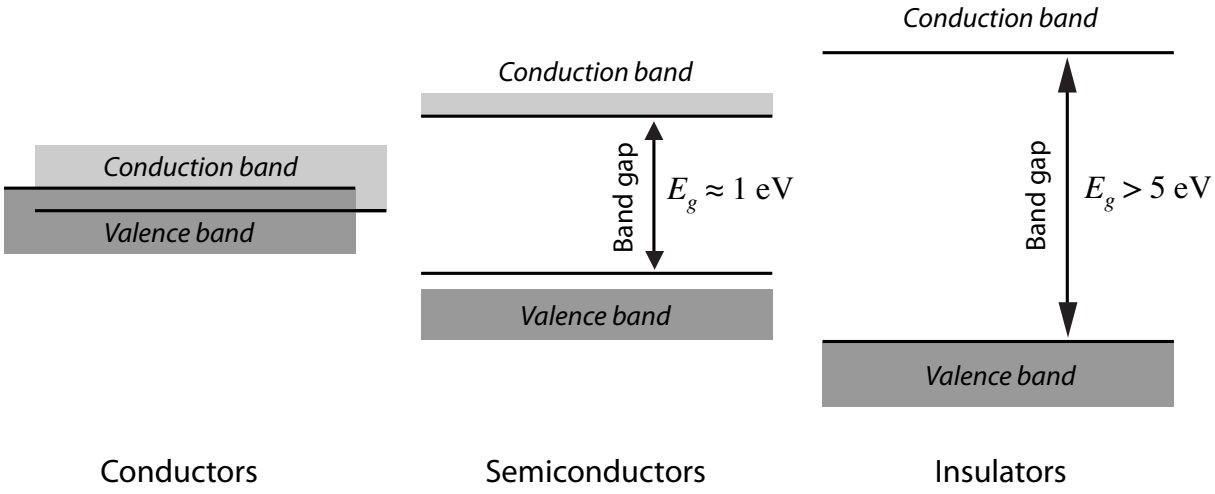


Figure 2.1: Energy bands
A schematic representation of the relative position of the edge of the valence and conduction band, in order of decreasing conductivity. Conductors have no area of disallowed states, whereas the valence and conduction band of insulators and semiconductors are separated by a forbidden zone: the band gap. At room temperature, valence electrons can be excited to the conduction band, leaving behind holes in the valence band.

concentration p are given by:

$$n = N_c e^{-\left(\frac{E_c - E_\mathrm{F}}{kT}\right)} \tag{2.2}$$

$$p = N_v e^{-\left(\frac{E_\mathrm{F} - E_v}{kT}\right)}, \tag{2.3}$$

where N_c is the effective density of states of the conduction band and N_v that of the valence band[2]. E_c is the energy of the lower edge of the conduction band and E_v that of the upper edge of the valence band.

Intrinsic semiconductors

A semiconductor with equal electron and hole concentration in thermal equilibrium,

$$n = p = n_i\,, \tag{2.4}$$

is called intrinsic, where n_i is the intrinsic carrier concentration. From Equations 2.2 and 2.3, it can be derived that the Fermi level of an intrinsic semiconductor is located in the middle of the band gap:

$$E_\mathrm{F} = E_i = \frac{E_c + E_v}{2} + \frac{kT}{2} \ln\left(\frac{N_v}{N_c}\right), \tag{2.5}$$

[2]For silicon at 300 K, N_c and N_v are $\sim 2.8{\cdot}10^{19}$ cm^{-3} and $\sim 1.8{\cdot}10^{19}$ cm^{-3}, respectively.

where E_i is called the intrinsic Fermi level.
An important relation that applies to any semiconductor in thermal equilibrium is that the product of the electron and hole concentration is constant and only depends on the width of the band gap and temperature:

$$np = n_i^2 = N_c N_v e^{-\left(\frac{E_c - E_v}{kT}\right)} = N_c N_v e^{-\left(\frac{E_g}{kT}\right)}. \tag{2.6}$$

If the concentration of one carrier type is larger than the equilibrium concentration, equilibrium will be restored through processes (see Section 2.1.3) that reduce the concentrations of either electrons or holes to maintain $np = n_i^2$. Note that this relationship does not depend on the Fermi level and therefore also applies to semiconductors in which one carrier type concentration exceeds the other: extrinsic semiconductors.

Extrinsic semiconductors

Intrinsic semiconductors only represent the ideal case of a pure and perfect crystal. The electron and hole concentrations are balanced and no excess of electrons or holes exist. In reality, there are almost always imperfections present in the semiconductor lattice which are introduced during the fabrication process.
Typical imperfections are atomic impurities and crystalline defects. Both introduce intermediate states in the band gap. Depending on their position relative to the intrinsic Fermi level, they fall in two categories: shallow-level and deep-level states. Shallow-level states are located no further than 0.1 eV from the band edges. If the difference is larger, i.e. the states are located deeper in the band gap, one speaks of deep-level states.

Shallow-level states Shallow states can be introduced by impurity atoms. Figure 2.2 shows shallow states at two different energy levels in the band gap and their influence on the conductivity of the semiconductor material.
Atoms that have more valence electrons than the atoms of the semiconductor crystal introduce electron-filled states of energy E_d close to the conduction band. Because of their close proximity to the conduction band, their ionisation probability is high and they can easily donate electrons to the conduction band. Logically, these impurity atoms are called donors. Atoms with fewer valence electrons introduce empty states just above the valence band, which can be filled easily by valence electrons. These states of energy E_a have a large probability of accepting electrons. This can be seen as if holes are added to the valence band. These impurity atoms are called acceptors. Extrinsic semiconductors having a majority of electrons are called n-type, and similarly, those having a majority of holes are called p-type. Logically, electrons in n-type material are called majority carriers and the holes are referred to as minority carriers. The opposite applies to p-type semiconductors.
Due to donor and acceptor states, the position of the Fermi level is shifted to one of the band edges. This shift is dependent on the donor and acceptor concentrations. The Fermi

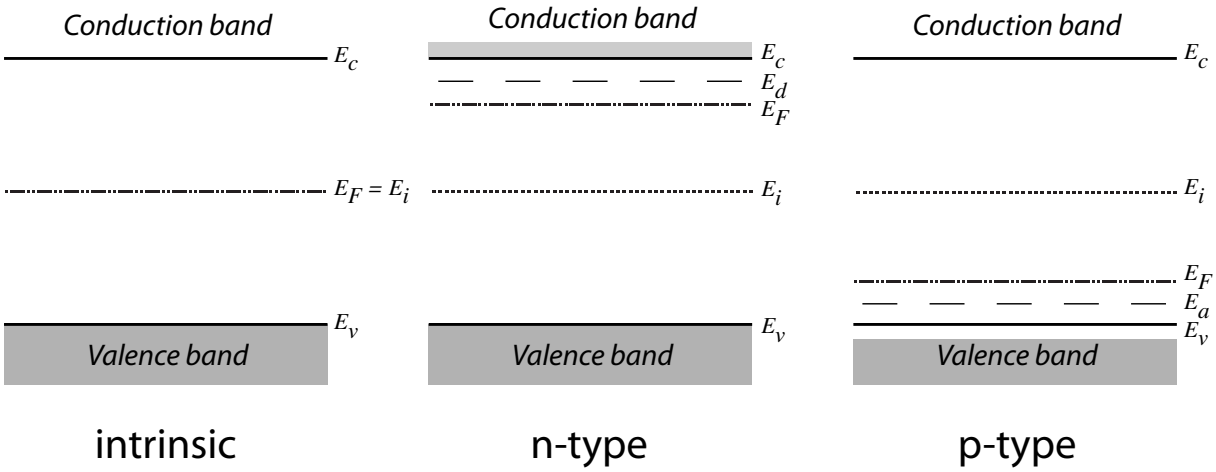


Figure 2.2: Intrinsic and extrinsic semiconductors
The band diagrams of both intrinsic and extrinsic semiconductors. The Fermi level of intrinsic semiconductors is located in the middle of the band gap. Donor and acceptor impurities introduce states that cause the Fermi level to shift to one of the band edges. Obviously, this alters the carrier concentration and thus the conductivity of the semiconductor. Donors make the semiconductor n-type, whereas acceptor-dominated semiconductors are called p-type.

level relative to the band edge becomes:

$$E_c - E_\mathrm{F} = kT \ln\left(\frac{N_c}{N_d}\right) \tag{2.7}$$

$$E_\mathrm{F} - E_v = kT \ln\left(\frac{N_v}{N_a}\right) . \tag{2.8}$$

From this, it can be seen that the Fermi level shifts towards the conduction band in the case of n-type semiconductors and towards the valence band in the case of p-type semiconductors.
Depending on the concentration of donors and acceptors, semiconductors are categorised into different types. These are listed in Table 2.1.

Deep-level states Deep-level states in the band gap have energies that differ more than 0.1 eV from the band edges. Typical deep states are introduced by metallic impurities or defects in the crystal lattice which can be caused by one of the fabrication steps. Lattice defects may consist of atomic dislocations, vacancies (i.e. lattice sites missing an atom) or interstitials (i.e. extra atoms between lattice sites). Two defects that are generally introduced during the growth of cadmium telluride are the cadmium vacancy and the tellurium interstitial.

Doping In contrast to what one would expect, it is very common in semiconductor device fabrication to introduce small and controlled amounts of impurity atoms. This

Table 2.1: Semiconductor classification in terms of donor and acceptor concentration levels.

Donor/acceptor concentration (cm^{-3})	**Type**
$\sim 10^{12}$	ν /π
$10^{13} - 10^{15}$	n^- /p^-
$10^{15} - 10^{17}$	n /p
$10^{17} - 10^{19}$	n^+ /p^+
$> 10^{19}$	n^{++}/p^{++}

process is called doping and the atoms added are named dopants. Dopants are used to manipulate the electrical properties of the material. One important reason is to negate the effects of unwanted impurities. If the donor and acceptor concentrations are equal, the extra electrons provided by the donor will fill the empty states of the acceptor, thereby cancelling out each other's influence. In this way, carrier concentrations can be restored to the intrinsic level. This resistivity tuning by free-carrier elimination is called compensation [31, 32].
Besides compensation of semiconductor bulk material, very local doping is done to manufacture electronic circuits as well sensor structures. This will be discussed in more detail in Sections 2.2 and 2.3.

2.1.3 Carrier generation and recombination

The process that involves creation of electron-hole pairs by exciting electrons from the valence band to the conduction band is called generation. This occurs, for example, when an X-ray photon interacts with the sensor. In this case, the number of generated electron-hole pairs N depends on the kinetic energy E_{kin} of the photoelectron and the average energy W needed to create an electron-hole pair:

$$N = \frac{E_{\mathrm{kin}}}{W}\,. \tag{2.9}$$

Values for W for the sensor materials studied are listed in Table 2.2 on page 29.
The reverse process is referred to as recombination. It involves the transition of an electron from the conduction band to the valence band and the subsequent annihilation with a hole. Either one of these processes occurs whenever the product of the electron and hole concentration deviates from the thermal-equilibrium situation: $np = n_i^2$. When $np < n_i^2$ thermal generation will restore the system to equilibrium, whereas if $np > n_i^2$ recombination occurs. Both generation and recombination can involve both direct and indirect transitions between the bands. Direct means that a valence electron is elevated to the conduction without involvement of any intermediate process. Indirect transitions, on the other hand, occur through intermediate states in the band gap. The direct transition

is known as the band-to-band generation-recombination process, whereas the indirect one is referred to as the intermediate-state assisted or Shockley-Read-Hall process [33]. Figure 2.3 shows a schematic representation of both direct and indirect generation and recombination processes.

Direct and indirect semiconductors

Depending on the relative position of the valence and conduction band in momentum space, semiconductors have either a direct or indirect band gap. To understand what determines this, the concept of crystal momentum of electrons in a crystal lattice has to be introduced. The underlying theory, however, is beyond the scope of this thesis. For direct band-gap semiconductors the crystal momentum of the maximum-energy state of the valence band matches that of the minimum-energy state of the conduction band, which makes that band-gap transitions only require energy transfer. In indirect semiconductors, however, the valence-band maximum does not match the conduction-band minimum, which requires momentum transfer in addition to energy transfer. This momentum transfer is mediated by lattice vibrations, also known as phonons.

Band-to-band transitions

Band-to-band generation requires the valence-band electron to gain enough energy to surmount the band gap. Next to thermal generation, valence-band electrons can be excited to the conduction band through interactions with photons or charged particles. Conversely, conduction electrons can recombine with holes and annihilate. In direct semiconductors, the recombination energy can be converted to a photon or transferred to an Auger electron. In the case of indirect semiconductors, the band-to-band transitions require the transfer of momentum in addition to energy transfer. These transitions can be promoted by intermediate states within the band gap through two or multiple-step transitions, commonly known as Shockley-Read-Hall transitions.

Shockley-Read-Hall transitions

In a perfect single-crystal semiconductor no levels exist within the band gap and only band-to-band transitions occur. In reality, as has been discussed, semiconductors are extrinsic. As a consequence, the intermediate states can act as stepping stones for generation and recombination, or trap charges. Four intermediate-state assisted processes can be distinguished:

1. Hole emission: This process involves the capture of a valence-band electron by the intermediate state. As this electron leaves behind a hole, it can be seen as if the gap state emits a hole.

2. Electron emission: The transition of a captured electron to the conduction band.

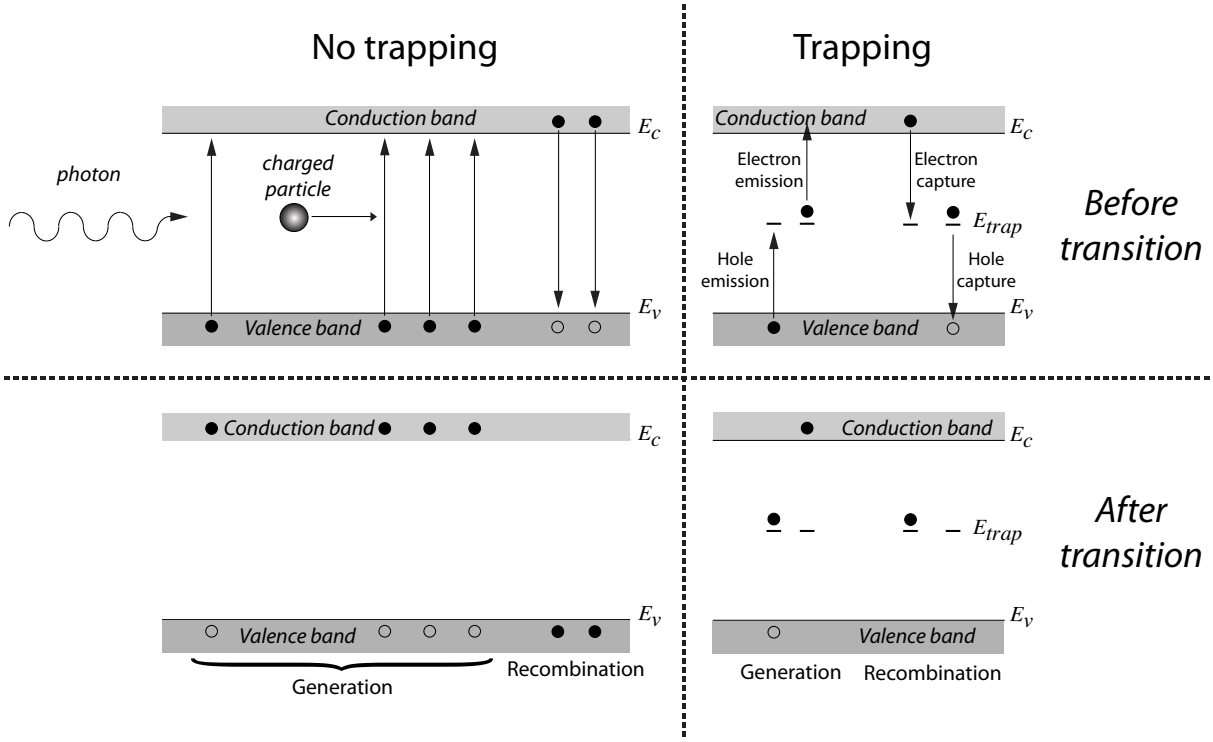


Figure 2.3: Generation and recombination
Generation and recombination processes involve both direct and indirect transitions. In addition to thermal generation, electrons can surmount the band gap when excited by photons or charged particles. Recombination is the process that involves the transition of an conduction electron to the valence band. Both generation and recombination involve direct and indirect transitions between the valence and conduction band. Indirect transitions occur via intermediate states that act as generation-recombination or trapping centres.

3. Electron capture: The process in which an electron from the conduction band is caught by a gap state.

4. Hole capture: The transition of a captured electron from a trap to the valence band, which can be seen as if a hole is captured by the intermediate state.

Emission processes 1 and 2 combine to generate electron-hole pairs, whereas the capture mechanisms 3 and 4 contribute to electron-hole recombination. In addition, a sequence of transitions 2 and 3 or transitions 1 and 4 can occur. In either case, a carrier is captured and subsequently emitted to the band where it came from and neither generation nor recombination occurs. This process is known as trapping and is predominantly mediated by shallow states. Due to their position close to the band edges, the capture probability of shallow states is high. Nonetheless, their emission probability is equally high, which means charge carriers only occupy these states for a relatively short time (of the order of ns). Deep states, however, have a considerably lower capture and emission probability.

Consequently, these states can trap carriers for a relatively long time ($0.1 - 1$ μs).

2.1.4 Carrier transport

As discussed in the previous section, pairs of electrons and holes are created by excitation of valence electrons to the conduction band. These charge carriers are free to move through the crystal and are therefore responsible for conduction. The two dominant mechanisms for charge-carrier movement are diffusion and drift. Consequently, the total current is composed of a drift current and a diffusion current.

To be able to consider electrons and holes as free charge carriers in a semiconductor crystal, the concept of effective mass has to be introduced. It reflects the influence of the periodic potential of the nuclei on the movement of the charge carrier with respect to its direction of propagation. It is commonly expressed as:

$$\frac{1}{m^*} = \frac{1}{\hbar^2} \frac{d^2E(k)}{dk^2}\,, \tag{2.10}$$

where m^* is the effective mass, $\hbar$ the reduced Planck's constant, $E(k)$ the energy-momentum dispersion relation and k the wave vector. The mean kinetic energy of the carrier in thermal equilibrium can be defined using the equipartition theorem:

$$\frac{1}{2}m^*\bar{v}_{\mathrm{th}}^2 = \frac{3}{2}kT\,, \tag{2.11}$$

where $\bar{v}_{\mathrm{th}}$ is the carrier's mean thermal velocity, k Boltzmann's constant and T the absolute temperature. In thermal equilibrium free carriers collide with the vibrating lattice atoms and with possible dopant atoms. This random thermal motion is characterised by the carrier's mean free path λ, which describes the mean distance travelled between two collisions:

$$\lambda = \bar{v}_{\mathrm{th}} \cdot \tau_{\mathrm{c}}\,, \tag{2.12}$$

where τ_{c} is the characteristic time between collisions. In thermal equilibrium the carriers are not immobile, but the average net movement is zero.

Diffusion

In a non-uniform charge-carrier distribution, i.e. when a particle locally creates a cloud of electron-hole pairs, concentration differences cause a net carrier flow with a flux that is proportional to negative of the concentration gradient. In other words, carriers will flow from high-concentration regions to low-concentration regions. The resulting flux is described by Fick's first law [34]:

$$\vec{\Phi}_n = -D_n\vec{\nabla}n \qquad\qquad \vec{\Phi}_p = -D_p\vec{\nabla}p\,, \tag{2.13}$$

where n and p are the electron and hole concentration and $\vec{\Phi}_n$ and $\vec{\Phi}_p$ are the electron flux and hole flux, respectively. D_n and D_p are the electron and hole diffusion coefficient. They

are a measure of the ease with which the respective carrier diffuses due to a concentration gradient. The resulting current-density components $\vec{J}_{n,p}^{\text{diff}}$ are given by the product of the electron or hole charge $\pm q$ and their respective flux $\vec{\Phi}_{n,p}$:

$$\vec{J}_n^{\text{diff}} = qD_n\vec{\nabla}n \qquad\qquad \vec{J}_p^{\text{diff}} = -qD_p\vec{\nabla}p\,. \tag{2.14}$$

The total current density due to diffusion is the sum of both the electron and hole current contribution:

$$\vec{J}^{\text{diff}} = \vec{J}_n^{\text{diff}} + \vec{J}_p^{\text{diff}} = qD_n\vec{\nabla}n - qD_p\vec{\nabla}p\,. \tag{2.15}$$

Drift

When a voltage is applied across a semiconductor, the resulting electric field $\vec{E}$ will exert a net force $\vec{F}$ on the free electrons and holes:

$$\vec{F} = \pm q\vec{E}\,. \tag{2.16}$$

Due to scattering processes, the charge carriers will accelerate to a mean speed, known as the drift velocity $\vec{v}_{n,p}^{\text{drift}}$. Assuming a constant electric field, it can be approximated as follows:

$$|\vec{v}_{n,p}^{\text{drift}}| \approx \frac{1}{2}|\vec{v}_{n,p}^{\text{final}}| = \frac{1}{2}\frac{|\vec{F}|}{m_{n,p}^*}\tau_c = \frac{q\tau_c}{2m_{n,p}^*}|\vec{E}| = \mu_{n,p}|\vec{E}|\,, \tag{2.17}$$

where $m_{n,p}^*$ denotes the electron's or hole's effective mass and $\mu_{n,p}$ is the electron or hole mobility, which is the proportionality factor (expressed in units of cm^2/Vs) between the electric field and its drift velocity. The carrier's mean drift length $L_{n,p}$, not to be confused with the mean free path λ, is determined by its mean lifetime $\tau_{n,p}$.

$$L_{n,p} = |\vec{v}_{n,p}^{\text{drift}}|\tau_{n,p} = (\mu\tau)_{n,p}|\vec{E}|\,. \tag{2.18}$$

Given an electric field, it means that the product of μ and τ determines the survival of the carrier during its drift towards the electrode. The $\mu\tau$-product is an important measure of the purity of the sensor, as it reflects the efficiency with which charge can be collected. Table 2.2 lists values of the $\mu\tau$-product and other fundamental parameters for high-quality crystals of the sensor materials studied in this thesis. For comparison, the values for amorphous selenium are given as well.

The current density due to drift can be expressed as the product of the charge concentration and the drift velocity:

$$\vec{J}_n^{\text{drift}} = -qn\vec{v}_n^{\text{drift}} = qn\mu_n\vec{E} \qquad\qquad \vec{J}_p^{\text{drift}} = qp\vec{v}_p^{\text{drift}} = qp\mu_p\vec{E}\,, \tag{2.19}$$

with the total current density being the sum of the electron and hole components.

$$\vec{J}^{\text{drift}} = \vec{J}_n^{\text{drift}} + \vec{J}_p^{\text{drift}} = q(n\mu_n + p\mu_p)\vec{E}\,. \tag{2.20}$$

The relation between the mobility and the diffusion coefficient is given by the Einstein relation [35]:

$$\frac{D_{n,p}}{\mu_{n,p}} = \frac{kT}{q}\,. \tag{2.21}$$

Table 2.2: Fundamental semiconductor-sensor parameters at 300 K. For comparison, also the values for amorphous selenium are given.

	Silicon	**Gallium arsenide**	**Cadmium telluride**	**a-Selenium**
Z	14	31; 33	48; 52	34
ρ (g/cm^3)	2.33	5.32	6.2	4.3
E$_g$ (eV)	1.12	1.42	1.56	2.3
W (eV)	3.61	4.26	4.43	$20-50$
R (Ωcm)	$< 10^4$	10^8	10^8 - 10^9	$\sim 10^{14}$
μ_n (cm^2/Vs)	1500	8500	1100	$3{\cdot}10^{-3}$
μ_p (cm^2/Vs)	450	400	100	0.12
τ_n (s)	$>10^{-3}$	$3{\cdot}10^{-6}$	$3{\cdot}10^{-6}$	$4{\cdot}10^{-4}$
τ_p (s)	$2{\cdot}10^{-3}$	$2{\cdot}10^{-8}$	$2{\cdot}10^{-6}$	$4{\cdot}10^{-5}$
$(\mu\tau)_n$ (cm^2/V)	>1	$3{\cdot}10^{-2}$	$3{\cdot}10^{-3}$	$1{\cdot}10^{-6}$
$(\mu\tau)_p$ (cm^2/V)	~ 1	$8{\cdot}10^{-6}$	$2{\cdot}10^{-4}$	$4{\cdot}10^{-6}$
D_n (cm^2/s)	39	220	28	$8{\cdot}10^{-5}$
D_p (cm^2/s)	12	10	2.6	$3{\cdot}10^{-3}$

Continuity equation

In the previous two sections, the diffusion and drift current were derived for both electrons and holes. The total electron and hole current can thus be expressed as follows:

$$\vec{J}_n^{tot} = \vec{J}_n^{\text{diff}} + \vec{J}_n^{\text{drift}} = \quad qD_n\vec{\nabla}n + qn\mu_n\vec{E} \tag{2.22}$$

$$\vec{J}_p^{tot} = \vec{J}_p^{\text{diff}} + \vec{J}_p^{\text{drift}} = \quad -qD_p\vec{\nabla}p + qp\mu_p\vec{E}\,. \tag{2.23}$$

Because charge is a conserved quantity, the time rate of change of the charge-carrier concentration ρ must be equal to the net current density $\vec{J}$ plus the net generation-recombination rate $(G-R)$. This relationship is described by the continuity equation:

$$-\frac{\partial\rho}{\partial t} = \pm q\frac{\partial(n,p)}{\partial t} = \vec{\nabla}\cdot\vec{J}_{n,p} + G_{n,p} - R_{n,p}\,. \tag{2.24}$$

Using equations 2.22 and 2.23 for the total current densities, the time rate of change of the electron and hole concentrations is described by the following relations:

$$\frac{\partial n}{\partial t} = \quad D_n\Delta n + \mu_n(\vec{E}\cdot\vec{\nabla}n + n\vec{\nabla}\cdot\vec{E}) + G_n - R_n \tag{2.25}$$

$$\frac{\partial p}{\partial t} = \quad D_p\Delta n - \mu_p(\vec{E}\cdot\vec{\nabla}p - p\vec{\nabla}\cdot\vec{E}) + G_p - R_p\,. \tag{2.26}$$

2.1.5 Signal formation

The former section discussed carrier transport. Both diffusion and drift cause charge-carrier movement. As soon as the generated charge carriers start to move and separate, a signal is formed on the collecting electrodes. This can be explained by using the method of mirror charges. The introduction of charge into a sensor volume changes the electric field inside. The electric field from the charge induces mirror charges on the electrodes, the magnitude of which changes as the carriers travel towards the electrodes. The induced charge itself cannot be measured, though its time-dependent change can. This change manifests itself as a current, the time integral of which equals the total induced charge.
Signal formation through current induction is treated by the Shockley-Ramo theorem [36], which states that the instantaneous current on a given electrode a can be expressed in terms of a weighting field $\vec{E}_w$:

$$i_a = -q\vec{v}_{n,p} \cdot \vec{E}_w \,, \tag{2.27}$$

where i_a is the instantaneous current, $\vec{v}_{n,p}$ the velocity of the charge carrier, which is determined by its mobility and the electric field. The net induced charge Q_a by a carrier moving from position x_1 to position x_2 on this electrode is determined by the difference between the (dimensionless) weighting potentials $(\phi_a(x_2) - \phi_a(x_1))$ at those positions:

$$Q_a = q(\phi_a(x_2) - \phi_a(x_1)) \,. \tag{2.28}$$

The unit of the weighting field is cm^{-1} and should not be confused with the electric (drift) field. Whereas the electric field determines the trajectory and velocity of the charge carrier, the weighting field only describes how charge motion couples to a specific electrode. For a homogeneous medium, it is only determined by the configuration and geometry of the electrodes disregarding the medium through which the carrier travels. It can be seen as the component of the electric field in the direction of the charge carrier's velocity, under the following circumstances: (i) both the medium and the charge are removed, (ii) the given electrode is raised to unit potential and all the other electrodes are grounded.
This definition implies that the only situation in which the electric field and the weighting field are equal, is the parallel-plate configuration. Figure 2.4 shows an example of two weighting-potential distributions together with the induced current and charge as a function of time for both a parallel-plate and a pixellated configuration. In the parallel-plate geometry the weighting potential is uniformly distributed, which causes both the electron and hole drift current to be constant in time until all the carriers are collected. Due to the lower hole mobility, the hole current signal is smaller and lasts longer. In the pixellated configuration the weighting potential increases as the distance to the electrode decreases. The charge carrier is therefore subject to an increasing weighting field as it moves towards its collecting electrode. When electrons are created close to the cathode and the signal is acquired at the anode, the induced charge and current signal increase only slowly when the electrons begin to move. As they approach their collecting electrodes, the coupling to the electrodes strongly increases, which makes that the largest part of the signal is formed close to the electrode. This effect is commonly referred to as the small pixel effect [37] and becomes stronger as the ratio between the drift length and the pixel dimensions increases.

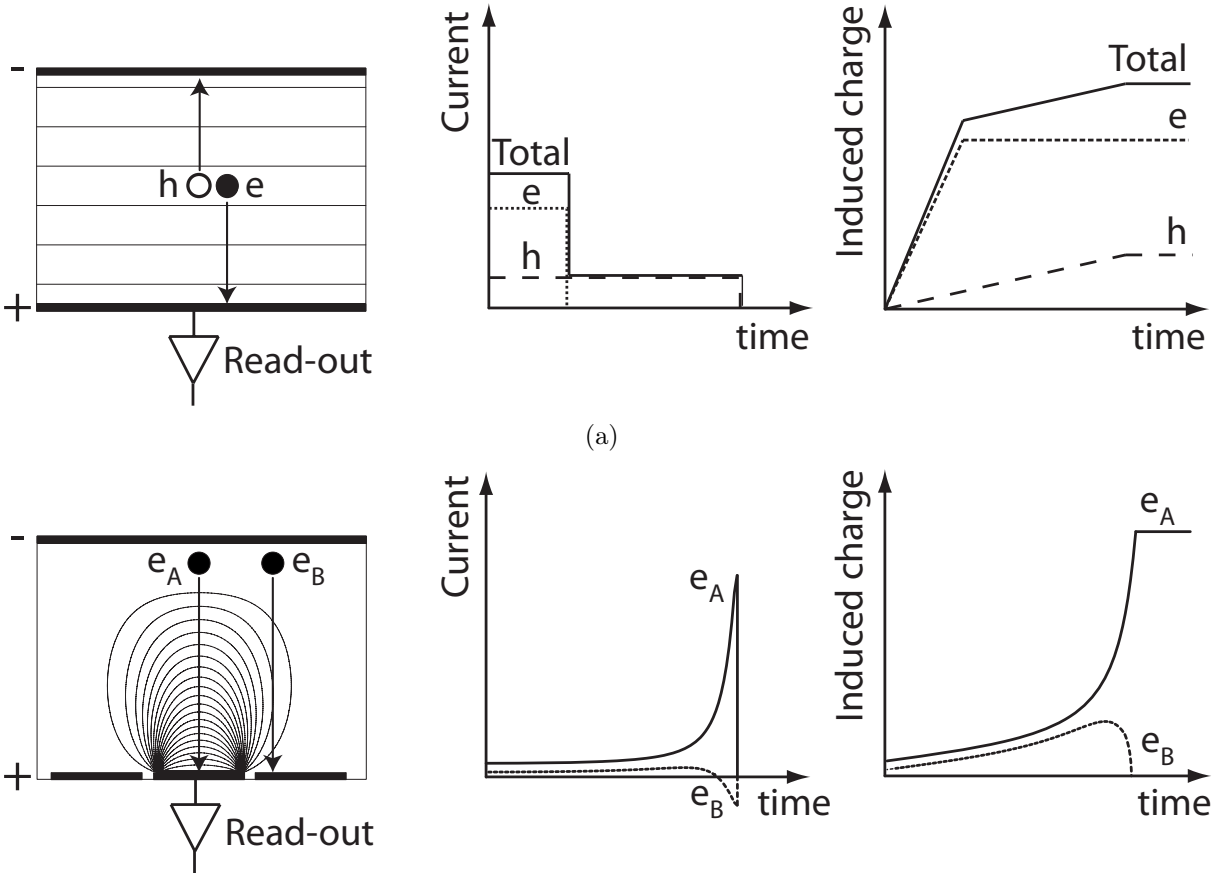


Figure 2.4: Weighting potential
The weighting-potential distributions for (a) a parallel-plate electrode configuration (simplified, I.e. assuming constant electric field) and (b) a pixellated one. The current signal and induced charge are dependent on the coupling of the carrier movement to a given collecting electrode. Figure based on [38].

Charge collection

In an ideal sensor, the total amount of induced charge is equal to the amount of charge deposited by the photon or charged particle. In reality, charge carriers have a finite lifetime and may recombine or get trapped during their travel towards the electrodes. The time a charge carrier can survive during its drift is therefore dependent on the concentration of trapping centres in the crystal. These centres reduce the amount of charge carriers available for signal formation. The remaining charge Q_{rem} relative to the total amount of generated charge Q_0 after a time t required to drift a distance x is given by:

$$\frac{Q_{\text{rem}}}{Q_0} = e^{-\frac{t}{\tau}} = e^{-\frac{x}{\mu\tau E}} . \tag{2.29}$$

For a parallel-plate configuration with a uniform electric-field distribution, it can be derived that the net amount of induced charge Q_{ind} can be expressed by:

$$\frac{Q_{\text{ind}}}{Q_0} = \frac{E}{d}\left[(\mu\tau)_n\left(1 - e^{-\frac{x_0}{(\mu\tau)_n E}}\right) + (\mu\tau)_p\left(1 - e^{-\frac{(d-x_0)}{(\mu\tau)_p E}}\right)\right] . \tag{2.30}$$

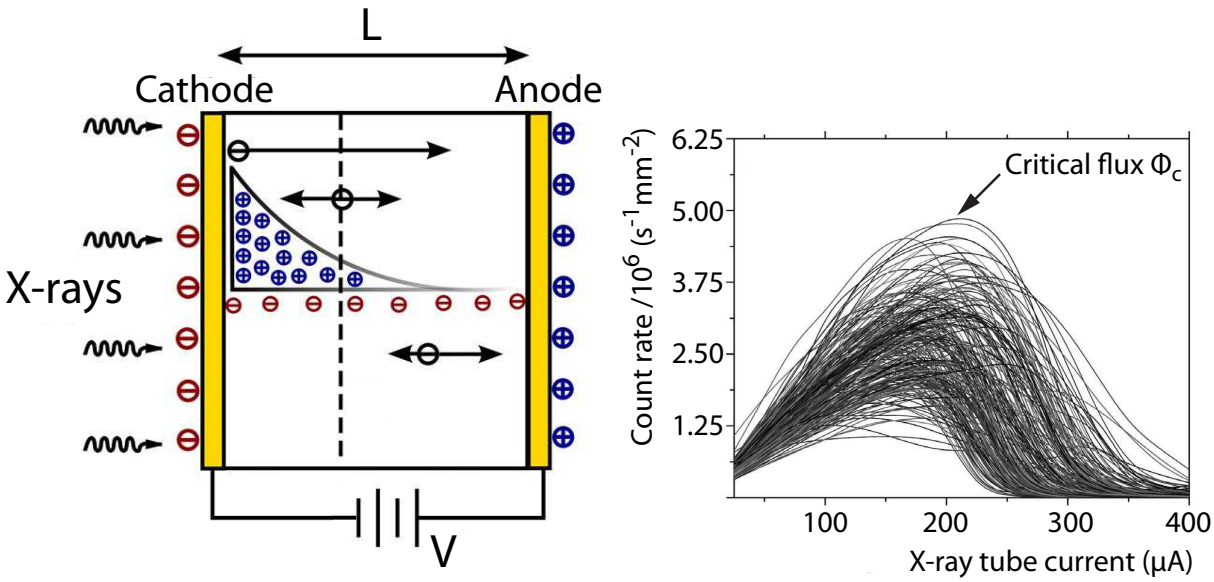
This relation is known as the Hecht equation [39] and describes the efficiency with which the charge carriers are collected. It is strongly dependent on the electric-field strength E, the product of the carrier mobility and lifetime ($\mu\tau$), and the mean drift length x_0 (or $(d - x_0)$ for opposite-sign carriers, where d represents the thickness of the sensor).
By measuring the total amount of induced charge at different bias voltages, this relation can be used to determine an approximate value for the $\mu\tau$-product of either holes or electrons for a given sensor material. This provides a measure of the purity and homogeneity of that specific material. In order to minimise the contribution of one of the two charge-carrier types, it is commonly ensured that the electron-hole pair creation is close to the electrode opposite to the electrode used to measure the signal. Then the Hecht relation reduces to:

$$\frac{Q_{\text{ind}}}{Q_0} = \frac{E}{d}(\mu\tau)_{n,p}\left(1 - e^{-\frac{d}{(\mu\tau)_{n,p} E}}\right) . \tag{2.31}$$

Polarisation An effect that reduces the charge collection efficiency and typically occurs in compound semiconductors is polarisation. It is regarded as the build-up of space charge in a crystal, which reduces the electric field and therefore results in a degradation of the detector's count-rate capability and energy response. It is believed that there are two mechanisms that cause polarisation:

1. Bias-induced polarisation [40–42]: at rectifying junctions, the band bending due to the applied potential can cause deep acceptor states (e.g. the cadmium vacancy in cadmium telluride) to cross the Fermi level, as a result of which they can get ionised. Consequently, space charge builds up, which leads to an overall reduction of the electric field across the sensor. This makes polarisation dependent on the type of electrodes used.

2. Radiation-induced polarisation [43–45]: this is schematically shown in Figure 2.5. Due to the relatively low mobility and short lifetime of holes in most compound semiconductors ($(\mu\tau)_{\text{p}}$ is in the order of 10^{-4} cm^2/V for cadmium telluride), their trapping probability is relatively high. This leads to an accumulation of holes close to the cathode, which locally shields the electric field. This shielding in turn reduces the drift velocity of the holes, which results in a further increase of the trapping probability. At a certain critical photon flux (typically of the order of $10^8 - 10^9$ photons s^{-1} mm^{-2} for good-quality cadmium telluride) the electric field is reduced to such an extent that the trapping probability is so high that more holes are trapped



(a) (b)

Figure 2.5: Polarisation
(a) A schematic representation of the build-up of positive space charge near the cathode. Accumulation of holes shields the electric field, which in turn reduces the drift velocity of the holes. (b) The measured photon flux as a function of the incoming photon flux for a polarising detector. At a certain critical photon flux the electric field collapses and charge collection becomes impossible. Figures from [44].

than de-trapped. At this point, the electric field collapses and charge collection becomes impossible.

2.2 Pixel structures

As discussed in Section 2.1.5, a carrier's drift time must be significantly shorter than its lifetime in order to be collected. A sufficiently high electric field must therefore ensure that charges are collected quickly. Due to the unavoidable presence of imperfections, a high electric field causes an non-negligible (generation) current flow in the sensor. Since this current has nothing to do with signal current, it is also referred to as dark current or leakage current. Leakage current is a source of unwanted shot noise that is superimposed on the signal and should therefore be minimised. To achieve this, semiconductors with a relatively low band gap, such as silicon, are processed to diode structures with rectifying contacts.

2.2.1 Diode structures

There are two common ways to realise diode structures: through the formation of a p-n junction or a surface barrier using Schottky-type contacts.

p-n junctions

A typical p-n junction [46–48] is formed by locally doping an n-type semiconductor with a high concentration of acceptor atoms. The energy-band diagrams of Figure 2.6 schematically show the rectifying properties of an abrupt p-n junction.
Due to a difference in carrier concentration, the holes of the p-type region diffuse into the n-type region and the electrons of the n region move towards the p region. As a consequence, excess electrons of the n region annihilate with excess holes of the p region (and vice versa), which leaves the donor and acceptor atoms ionised. In this way, a negatively charged region is formed at the p side of the junction, and similarly a positively charged area on the n side. As a result, a region free of charge carriers forms around the junction: the depletion region. The width of the depletion region depends on both the acceptor and donor concentration. The space charge forms a potential barrier for the excess electrons and holes, as a result of which diffusion and thus barrier growth stops. This barrier is known as the built-in potential V_{bi}.

Reverse and forward bias By externally applying a potential difference V_{bias} across the p-n junction, the depletion region can either be increased or reduced. Applying a reverse bias voltage, i.e. creating an electric field in the direction of the built-in field, causes the electrons and holes to be pulled away from the junction. This widens the depletion region and that is exactly what semiconductor sensor operation is based on. The depletion region is devoid of free carriers and forms a capacitor together with the p and n regions as electrodes. At the same time, the reverse potential provides a drift field for the generated electron-hole pairs. In this way, the p-n junction diode forms an ionisation chamber.
In the case of a highly p-doped abrupt p-n junction, i.e. only a negligibly thin slice of the p region is depleted due to the many holes available, the depletion region predominantly grows in the least doped region, the width of which can be approximated by:

$$W_{\mathrm{dep}} = \sqrt{\frac{2\epsilon_r\epsilon_0(V_{\mathrm{bi}} - V_{\mathrm{bias}})}{qN}}\,, \tag{2.32}$$

where V_{bias} is assumed negative, W_{dep} is the width of the depletion region, $\epsilon_r\epsilon_0$ is the permittivity of the semiconductor and N is the doping concentration of the bulk. The capacitance of the depleted volume with electrode area A can therefore be expressed as:

$$C = \frac{\epsilon_r\epsilon_0 A}{W_{\mathrm{dep}}} = A\sqrt{\frac{\epsilon_r\epsilon_0 qN}{2(V_{\mathrm{bi}} - V_{\mathrm{bias}})}}\,. \tag{2.33}$$

Under forward bias, the created electric field counteracts the built-in potential barrier. As a result, conduction-band electrons of the n region can easily reach the conduction

band of the p region, e.g. current can easily flow, provided that the forward bias voltage exceeds the built-in potential. For silicon diodes the built-in voltage is typically about 0.7 V.

Schottky contacts

Another way to realise rectifying structures, is to form a metal-semiconductor barrier contact, also referred to as Schottky contact [49]. For n-type semiconductors, this is achieved by depositing a metal with a work function that exceeds that of the semiconductor. Figure 2.7 shows this in terms of the energy-band diagrams before and after the materials are brought in contact.
Again, the difference in Fermi level causes band bending and thus a potential barrier for the majority carriers when both are brought in close contact. This barrier is known as the Schottky barrier ϕ_{barr} and is defined as the difference between the metal work function ϕ_m and the electron affinity χ of the semiconductor:

$$\phi_{\text{barr}} = \phi_m - \chi \,. \tag{2.34}$$

The built-in potential V_{bi} equals the difference between the Schottky barrier and the electron potential at the Fermi level in the semiconductor ϕ_s:

$$V_{\text{bi}} = \phi_{\text{barr}} - \phi_s \,. \tag{2.35}$$

Ohmic contacts

To bias the sensor, the structure must be connected to the outside world via low-resistance contacts, so called Ohmic contacts. From Equation 2.34, it can be seen that the barrier height is not dependent on the doping concentration and can therefore easily be varied by using metals with an appropriate work function. Ohmic contacts can be realised by depositing a metal with a work function that is smaller than that of the semiconductor, as a result of which the majority carriers of the semiconductor don't experience a barrier when trying to enter the metal. However, this is not entirely true, because it turns out that intermediate states at the surface of the semiconductor have a stronger influence on the barrier height than the work function of the metal. This makes it therefore hard to manufacture Ohmic contacts with the desired electrical behaviour. The barrier width, however, can be controlled by altering the doping concentration of the semiconductor. In this way, majority carriers can tunnel through the barrier, a phenomenon that is often referred to as field emission.

2.2.2 Ohmic structures

Diode structures can only operate under reverse bias, which makes that only one carrier type can be collected at the pixel electrode. Compound semiconductors, like gallium arsenide and cadmium telluride, have a wider band gap and therefore a higher intrinsic

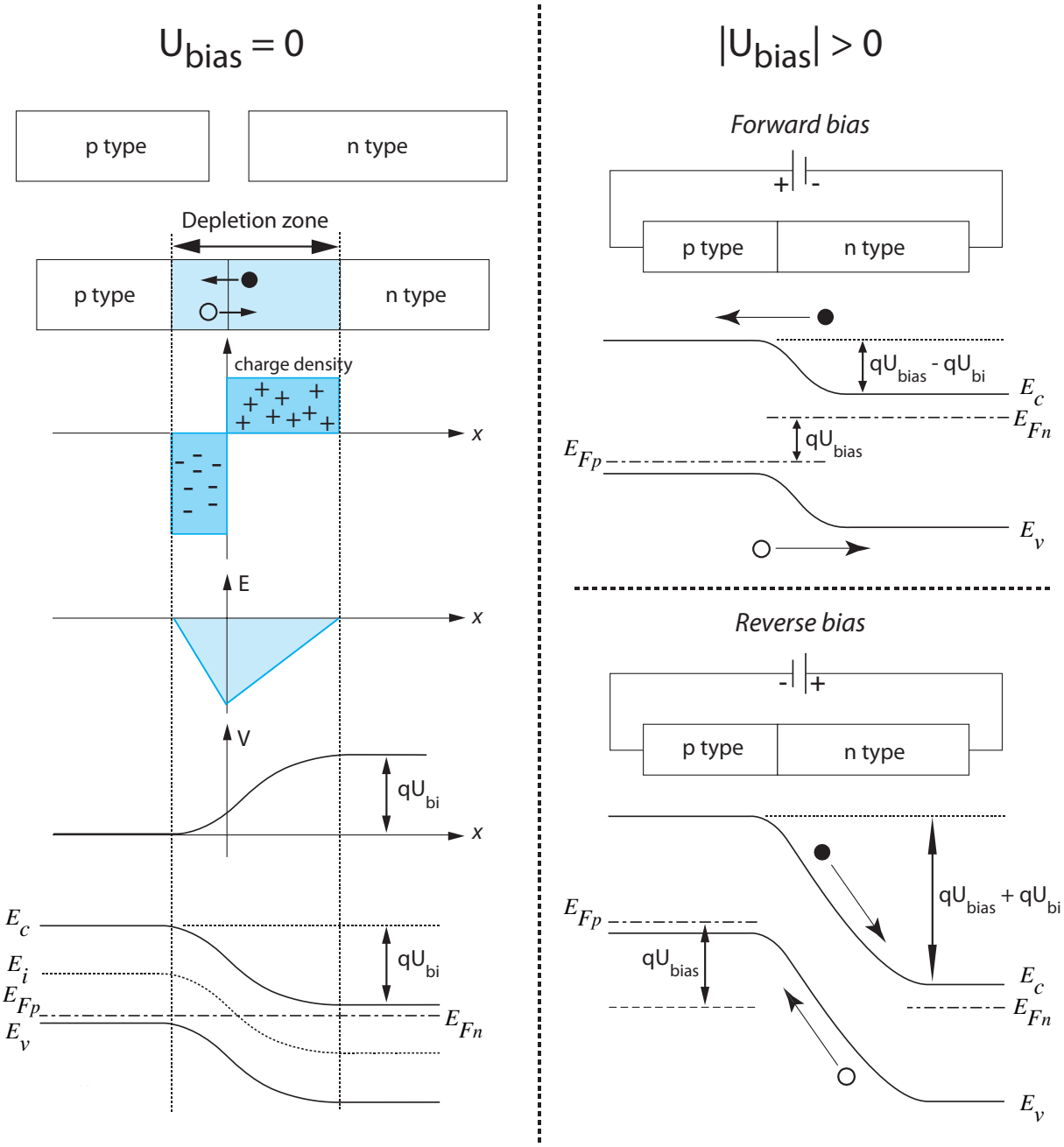


Figure 2.6: p-n junction
A p-n junction is formed by heavily doping a n-type semiconductor with acceptor atoms. Due to the difference in electron and hole concentrations of the two individual regions a potential barrier is formed by a region depleted of free carriers around the junction. This depletion region can either be expanded or reduced by applying a reverse or forward potential across the junction. A p-n junction is therefore a rectifying junction: current can only flow in one direction.

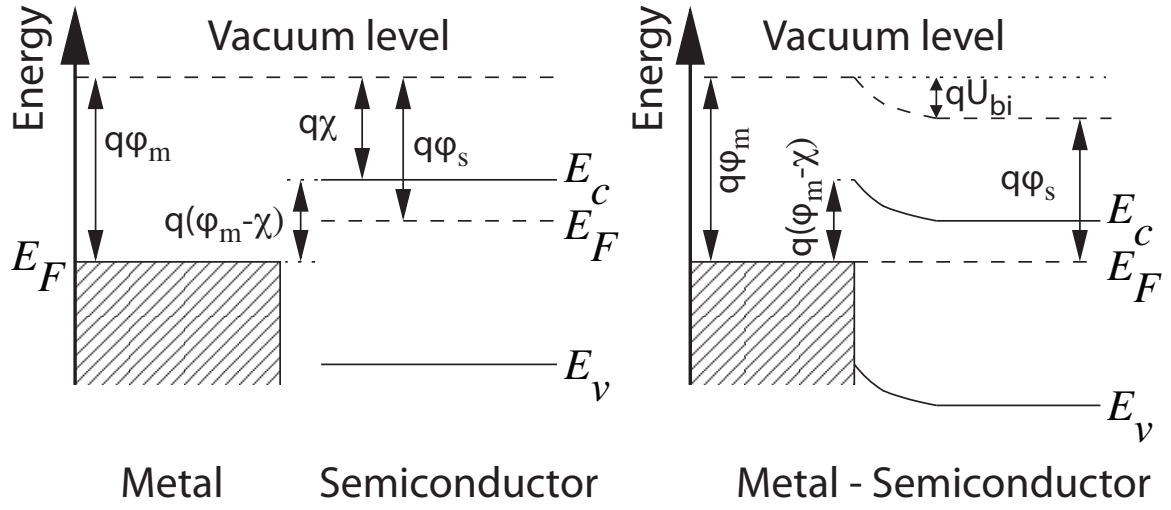


Figure 2.7: Schottky contact
A metal-semiconductor Schottky contact is formed when the work function of the metal exceeds that of the semiconductor. When they are brought in contact the original difference in Fermi level between them, causes a potential barrier for electrons, the Schottky barrier. Figure based on [50].

resistivity. These semiconductors are suitable for the use of Ohmic contacts without any rectifying junction. Use of Ohmic contacts allows for choosing which charge carrier to collect at the anode or cathode.

2.3 Sensor fabrication

The manufacturing of semiconductor sensors is a process that involves many steps [51]. First, single-crystal semiconductor material is grown in the form of a cylinder, called ingot. Subsequently, the ingot is sliced into circular wafers, which serve as the substrate material for the sensor. The substrate is then processed in order to realise patterned structures with the desired electrical properties. Patterning involves many steps, each of which will be briefly discussed hereafter. After pattering, the wafer is diced into smaller pieces to match the dimensions of the read-out chip. Dicing is an important step in the fabrication process of edgeless sensors, as it may introduce damage and contamination to the edge. Both can severely affect the sensor's performance.

2.3.1 Crystal growth

A common method for growing crystalline semiconductor material is the Czochralski technique [52]. A small piece of single-crystal material is brought into contact with its liquid-phase counterpart, which are respectively referred to as the seed and the melt. The seed is cooled and slowly pulled from the heated melt, as a result of which solidification

occurs at the solid-liquid interface. Commonly, the seed is slowly rotating as well. It thereby stirs the melt and ensures a uniform temperature at the interface. The crystal grown by this process has a cylindrical shape and is called ingot. Although the Czochralski method provides silicon of acceptable purity levels for electronic circuits, for sensors the ingot is often purified to obtain even better quality. These techniques are collectively called zone refining [53]. Nowadays, detector-grade silicon ingots with a diameter of up to 300 mm can be produced. This is not the case, however, for crystalline compound semiconductor materials. Their growth is more complicated and less under control. Consequently, only ingots of smaller dimensions can be grown. Typical maximum diameters are 150 mm for gallium arsenide and 75 mm for cadmium telluride. Due to mechanical and thermal differences between the individual elements that make up the crystal, dislocations and defects are easily introduced during growth. Two common growth methods are the Bridgman technique and the Travelling Heater Method [54, 55].

After growth, the ingot is sliced into circular wafers, which are subsequently prepared for processing. Wafer preparation includes lapping to make it of uniform thickness, chemical etching to clean it and polishing to smoothen it. The resulting product is called the substrate material, which forms the basis for further processing of desired electronic structures.

2.3.2 Processing

Figure 2.8 shows the main process steps for manufacturing pixel structures on silicon substrate material. Each step will be discussed in the upcoming sections.

Oxidation

The processing of substrate materials starts with the formation of a layer of thermally grown SiO_2 in the case of silicon. That is because its di-electric properties offer an excellent base for further processing as well as a number of other benefits to the performance of the final device:

- It is a good insulator: its resistivity is of the order of $10^{14} - 10^{16}$ Ωcm.
- Its growth provides a clean interface with silicon.
- It can be etched with solvents that leave silicon unaffected.
- It is a diffusion barrier for many dopant atoms.

In the case of compound semiconductors, oxides do not play a significant role. The oxides are of worse quality and commonly they cannot be produced using a simple oxidation process.

Patterning

Often, numerous sensors are manufactured on one wafer. Their dimensions, layout and position on the wafer are determined and realised by a process called patterning, which includes several processing steps. Commonly, there is space left in between the individual structures in order to provide some margin for separating the dies from each other. This margin is often referred to as the dicing street.

Photolithography First, a thin layer of photosensitive material, the photoresist, is applied to the oxidised surface. The pattern is transferred to the substrate using a mask with the desired layout, which is aligned to and held closely above the wafer. By exposing the uncovered parts to e.g. ultraviolet light, the photoresist becomes more or less soluble, depending on whether a positive or negative photoresist is used, respectively. A developer solution removes the more soluble parts, resulting in a pattern that corresponds to either the exposed or non-exposed parts of the photoresist. This process is called photolithography.

Etching Once the photoresist is patterned, the wafer is placed in an ambient that etches the exposed silicon-oxide or other type of insulation layer without affecting the photoresist. Afterwards, the resist is stripped off using solvents for example. What remains is a positive or negative oxide image of the mask.

Doping In the case of p-n junction diodes, the pattern allows for doping the parts that are not covered by the oxide layer. Introduction of p-type (e.g. boron) or n-type (e.g. phosphorus) dopants is commonly achieved using either diffusion or ion implantation.
Doping by diffusion is accomplished by exposing the wafer to e.g evaporated source of dopant atoms. Subsequently the wafer is heated up in order to enhance the diffusion of the impurity atoms into the substrate material.
A more common doping technique used today is ion implantation. This method uses an ion beam to introduce the dopant atoms. A distinct advantage of ion implantation is that the depth and profile of the implant can be controlled accurately. In addition, the ion dose is of excellent uniformity over large areas, which provides minimal variation in the doping concentration. On the downside, the method introduces point defects such as vacancies and interstitials. Possible damage can be recovered by thermal annealing, which is a heat treatment that allows the interstitial atoms to fill the vacancies. It can be seen as a re-crystallisation process.

Metallisation After doping, contact with the outside world is established by depositing metal contacts. Two techniques are most often used: physical vapour deposition and chemical vapour deposition. Both techniques involve the deposition of thin films.
Physical vapour deposition is based on the condensation of a vaporised form of the material to be deposited. A common physical-vapour-deposition technique is sputtering.
In chemical vapour deposition the wafer is exposed to one or more gases that react with, or decompose on the surface to form a film of the deposit.

A common contact metal used for silicon sensors is aluminium. Depending on the desired current-voltage behaviour, contacts for cadmium telluride sensors can be made of platinum, gold or indium.

Passivation Once the metal contacts are realised, a passivation material (e.g. silicon nitride) is deposited to protect the structure against damage and contamination. For hybrid pixel detectors, it is important that this layer protects the sensor from the chemicals used in the bump-bonding process.

The number of process steps to fabricate a silicon sensor is typically about 20 to 30.

2.3.3 Dicing

After the build-up of several patterned layers, the individual sensors are separated from each other by splitting the wafer up into smaller autonomous units. This process is known as dicing and can be done in several ways. Dicing is a crucial step in the manufacture of edgeless sensors, as it can strongly degrade the sensor's performance at the edge. Nowadays, there are several dicing options, three of which will be discussed in the upcoming sections.

Blade dicing

The most common method used today is diamond-blade dicing [56]. The method uses a rotating circular metal blade with diamond particles on its surface. The cutting edges of the particles allow for cutting through almost any type of material. Due to the wide variety of blades, it provides the possibility to control the kerf width, depth and straightness. Hence, it can be used for many types of structures of different thickness. The main drawback of blade dicing is the mechanical load on the wafer. Though the load can be controlled to some extent, its deleterious effects cannot be eliminated entirely. Figure 2.9 shows the main adverse effects:

- Micro-cracks at the edge side-wall, which can extend tens of microns into the structure.
- Chip-outs at the front and back side of the wafer.
- Edge contamination due to material stacking in the dicing street (i.e. passivation material and metal), blade dirt and water used for cooling the blade.

One solution is to use serrated blades. This significantly reduces the load on the water and provides better cooling. The kerf width is not as accurate as with regular blades though.
Blade dicing requires a relative wide dicing street (of the order of 100 µm), which reduces the wafer area available for structure fabrication. The area loss is only significant, however, for the fabrication very small devices like integrated circuits.
Blade dicing can only be used for straight dicing streets.

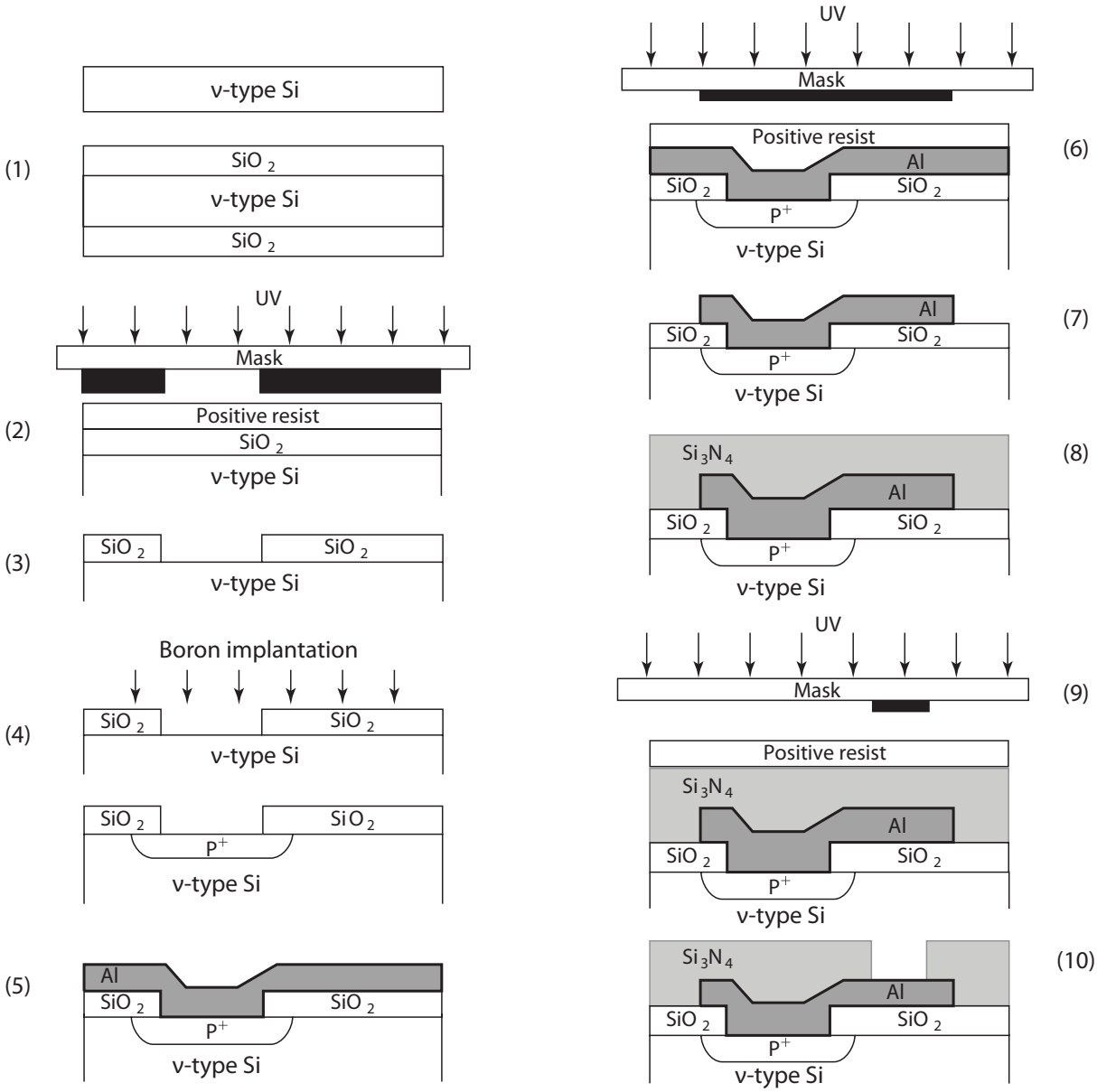


Figure 2.8: Fabrication steps
The fabrication of pixellated semiconductor sensors involves many steps. The main steps are shown for a typical silicon-sensor pixel: (1) oxidation, (2) photolithography, (3) oxide etching and photoresist removal, (4) pixel implantation / doping, (5) aluminium deposition, (6) photolithography, (7) aluminium etching and photoresist removal, (8) deposition of silicon nitride for passivation, (9) photolithography and (10) passivation etching for contact openings.

Laser dicing

Laser ablation Laser ablation is a process that involves the removal of wafer material by irradiation with laser pulses. These pulses locally generate a combination of melt and vapour. The vapour pressure drives the molten material out, as a result of which a kerf is created. The method is comparable to blade dicing in terms of edge smoothness. Although the kerf parameters can be optimised by tuning the wavelength, power and pulse duration of the laser, the resulting cut contains imperfections and contamination due to recast and debris. Also, the street width needed is non-negligible. The main advantage of laser ablation is the high removal rate and thus the short time it takes to dice a complete wafer.

Stealth dicing A method that enables to reduce the cutting waste and does not require post-cleaning is stealth dicing. Figure 2.9 shows the principle of this sub-surface dicing method. It involves the very local modification of the crystalline structure by focussing infrared laser light inside the wafer. The altered mechanical properties of this layer allow for accurate die separation by breaking using a tape-expansion technique. This minimises the transversal crack propagation, which results in a much smoother and cleaner edge. Moreover, the process speed of stealth dicing does not influence the edge quality as much as blade dicing does. Summarising, stealth dicing has the following main advantages over conventional dicing techniques:

- High-quality edge side-walls, as it is a dry and chipping-free process it provides smooth and clean edges.
- High-speed dicing possible.
- Low kerf loss, which allows for narrow streets (of the order of 10 µm) and thus higher wafer production yield.

The main limitations of stealth dicing are:

- It cannot penetrate metals or passivation material, which makes that the dicing street should be devoid of materials other than the semiconductor.
- The crystal orientation must allow for breaking along the modified layer.
- The maximum wafer thickness is limited. This due to the transmittance of the laser.

Plasma dicing

Another alternative is plasma dicing [58]. It involves etching by bombardment of ions accelerated by an electric field. This technique stems from MEMS[3] technology. It is an anisotropic process and therefore enables to create high aspect-ratio structures. It provides clean edges and moreover it can be easily implemented in the fabrication process. One

[3]Micro-Electro-Mechanical Systems

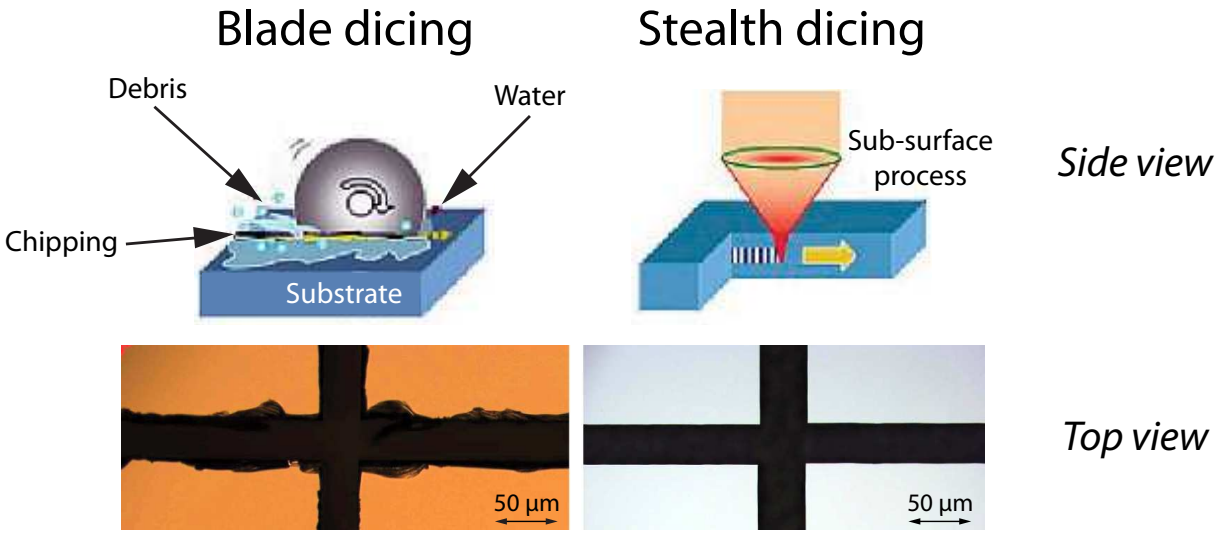


Figure 2.9: Dicing methods
Although blade dicing allows for cutting through almost any type of material, it causes chipping, contamination and micro-cracks at the edge's side-wall. A good alternative for thin wafers is stealth dicing: it provides high-quality edge side-walls with almost no kerf loss (a dicing-street width of 10 µm is already sufficient). The edge roughness resulting from either method is compared in the two bottom pictures. The gap between the stealth-diced dies is not because of kerf loss, but due to the tape expansion. Figures from [57].

example plasma-dicing technique is deep reactive ion etching, which is a derivative from reactive ion etching [59–61].
In reactive ion etching, a mixture of gases is used, only a part of which is ionised. In other words, the mixture is both chemically and physically active. Chemical action is isotropic, whereas the physical action is strongly directional, determined by the electric field in the plasma sheath above the wafer.
The physical action is typically preferred. However, the chemical action is also always present. Therefore, most of the time also a passivating component is included in the gas mixture. This passivating component does not remove material, yet deposits uniformily on the side-walls of the structure being etched. It then acts as a barrier for the chemically active components in the plasma. At the bottom of the structure, the ion bombardment removes this barrier, thereby continuously exposing the silicon to the etching plasma. With the right equilibrium of processing conditions, perpendicular sidewalls can be obtained with minimal undercut under the masking layer.
An improvement to reactive ion etching is deep reactive ion etching. The process is schematically shown in Figure 2.10. With deep reactive ion etching, the process continuously switches between etching and passivation, using two different gas mixtures and bias conditions. It provides more parameters to tune and therefore allows optimization of each individual step. This process is called the Bosch process [62] and typically results in scallops along the side-walls. The etching component typically comes from radicals of the

SF_6 molecules. A common passivating component is C_4F_8.
A distinct difference with other dicing techniques is that all dies can be separated at once.

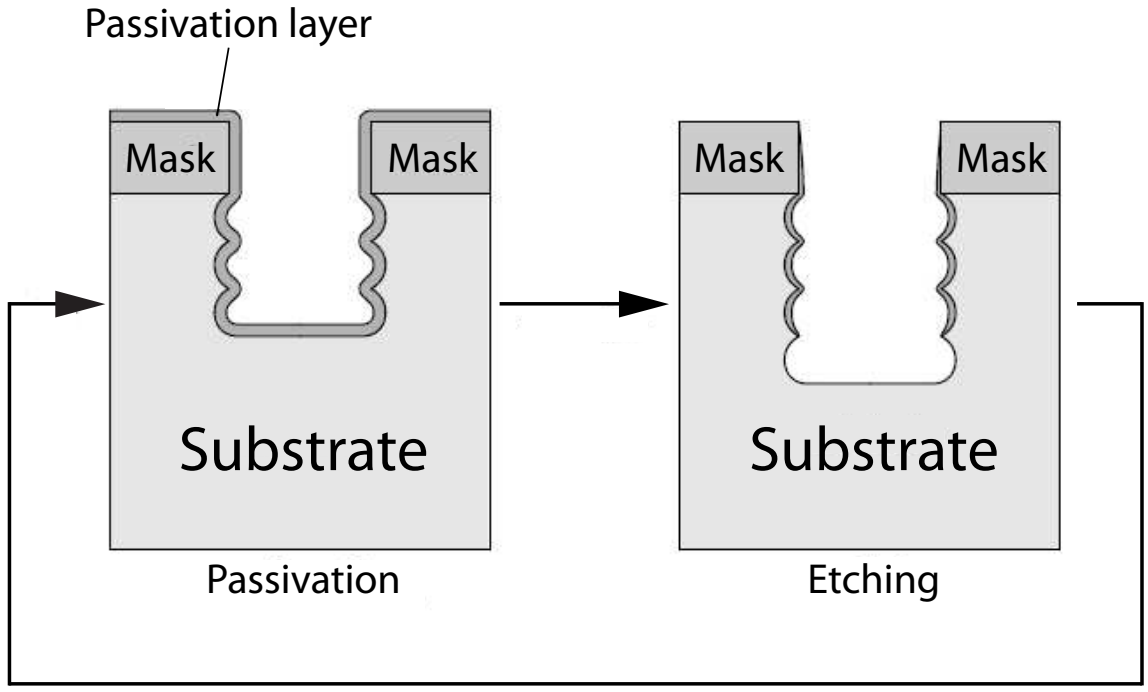


Figure 2.10: Deep reactive ion etching
Deep reactive ion etching provides clean edges and can be easily implemented in the sensor fabrication process. A typical deep-reactive-ion-etching technique is the Bosch process. The switching between etching and passivation results in scallops along the depth of the side-walls.

2.4 Sensor designs

Conventional sensors have guard electrodes around their active area to protect the pixel matrix from unwanted edge effects, which can have a width of up to a millimetre. Today, more and more applications demand near-edge sensitivity. A design change is therefore needed. Before evaluating the various options to fabricate edgeless sensors, two common types of conventional structures are described. Specifically, the effects that imperfect edges can have on the sensor's performance are discussed.

2.4.1 Conventional sensors

As discussed in Section 2.2.1, semiconductors with a moderate resistivity are commonly processed to diode-like sensor structures. In that case, either the back plane or each

pixel of the matrix forms a p-n junction or Schottky contact with the semiconductor substrate. Figure 2.11(a) depicts schematic cross-sections of two different p-n junction silicon structures. The most common silicon sensor is the p-in-n structure. A matrix of p^+-type pixel electrodes is realised by patterned implantation of boron atoms in an ν-type substrate. Hence, each pixel forms a p-n junction with the substrate. The back plane is unstructured and forms an n^{++}-type Ohmic contact with the substrate by heavily doping it with phosphorus.

A different approach is the n-in-n structure. In this case, the pixels are n^{++}-type

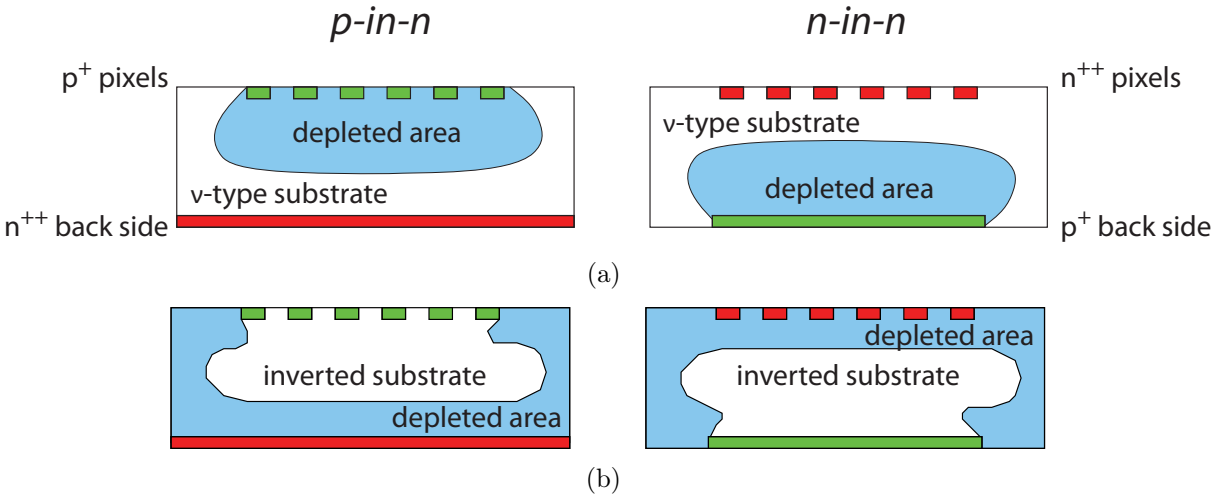


Figure 2.11: Implanted-junction structures
(a) Two common implanted-junction silicon sensors are the p-in-n and n-in-n structure. p-in-n structures are the most common approach of fabricating silicon sensors. If radiation damage is an issue, however, n-in-n sensor are more favourable. (b) Radiation-induced type inversion of the substrate causes the depleted area to grow from the side opposite to the original junction. Figure based on [50].

and the back plane is p^+. For p-in-n structures, the depleted area grows from the pixel matrix as the reverse bias voltage increases. For n-in-n structures, however, the depletion zone originates from the back plane. This requires a reverse bias voltage that depletes the entire sensor volume up to the pixel matrix. Otherwise, charge would be spread over many pixels, which implies a loss in resolution. However, the advantage of n-in-n sensors is their better radiation hardness. Radiation typically introduces defects that alter the substrate's effective doping concentration to more p-type, i.e. the bulk shows type inversion. As shown in Figure 2.11(b), the junction of n-in-n sensors will start to grow from n^+-type pixel matrix when the sensor is damaged by radiation. This allows for under-depleted operation, whereas for type-inverted p-in-n sensors the depletion region grows for the back side and hence the bias voltage has to be high enough to deplete the sensor over its full thickness. Consequently, for n-in-n sensors the applied bias voltage can still be of acceptable levels, whereas for p-in-n sensors the voltage must be increased more and more. Otherwise, like non-damaged n-in-n sensors, charge will be induced on

neighbouring pixels, which negatively affects the resolution and noise.
The main drawback of n-in-n sensors is that the process is much more complex and therefore more expensive. Since the junction grows from the back side, the back electrode must not be in contact with the edge of the sensor, which requires back side patterning. Moreover, due to electron accumulation underneath the inter-pixel oxide layers, n^{++}-type pixels must be actively isolated from each other by highly doped p-type regions.
An interesting radiation-hard alternative is the n-in-p sensor, whose potential is under study by the RD50 collaboration at CERN [63].

2.4.2 Edge effects

An important issue for almost every single-crystal semiconductor sensor is the edge. Several factors make it imperfect, each of which causes a reduction of the sensor's performance:

- At the surface and edge of the sensor the periodicity of the crystal lattice is abruptly terminated. This causes dangling bonds, which introduce a wide distribution of intermediate states in the band gap known as surface states. As the carrier lifetimes depend on the concentration of generation-recombination centres, generation currents can be considerably increased at the edge under reverse bias.

- Dicing, especially blade dicing, introduces damage and contamination at the edges (see Section 2.3.3). This damage manifests itself as micro-cracks propagating into the crystal, and chip-outs at the front and back sides. Micro-cracks reduce the crystalline integrity and increase the concentration of intermediate states in the forbidden gap. Both chip-outs and surface roughness of the edge side-wall are fertile ground for contamination and moisture, which function as excellent media for leakage paths. As a result, there can be a considerable current flow on the surface of the sensor's edges and corners.

- Due to the abrupt ending of the electric field along the outside of the pixel matrix, the field strength can be increased significantly close to the outer pixel electrodes [64, 65]. This can cause early break-down of the device.

As shown in Figure 2.12, these issues are dealt with by implanting one or multiple guard-ring electrodes around the pixel matrix [50, 66]. They gradually reduce the electric field towards the edge and prevent charge carriers generated at the edge from reaching the depletion region. As the potential difference between the front and back side is terminated, i.e. the outermost guard ring is at the same potential as the back side, surface currents that may flow along the edge towards the pixel matrix are reduced. The number of guard rings, and thus the width of the buffer zone between edge and pixel matrix, depends strongly on the required bias voltage. This periphery can be twice as wide as the thickness of the sensor. Sensors that operate in radiation-harsh environments need guard ring structures that are even wider (up to 1 mm for 300 µm thick sensors). The radiation requirement does not hold for imaging detectors, yet guard rings do take up a substantial fraction of the sensor's total area. In a tessellation of detector modules this will show up as

unwanted seams in the image. To reduce the sensor's inactive periphery, both slim-edge and active-edge sensors are under study nowadays.

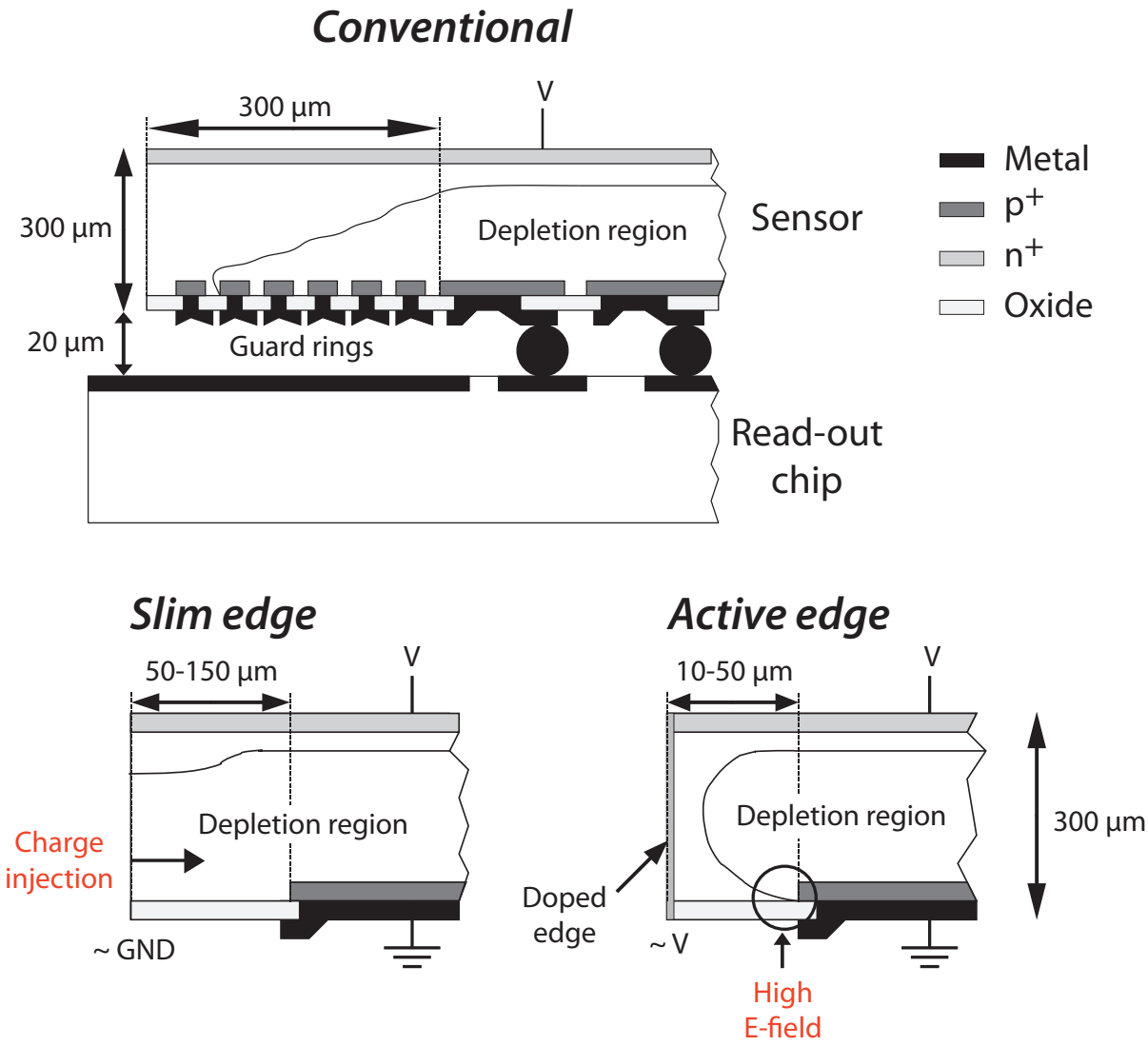


Figure 2.12: Edge processing and topology
A conventional sensor has guard rings that protect the active pixel region from unwanted edge effects. In a tessellation of detectors, this excess of material at the periphery shows up as seams. To reduce the distance between the active area and physical edge significantly, both active-edge and slim-edge sensors are being developed. Figure based on [50].

2.4.3 Edgeless sensors

To allow for a reduction of the insensitive periphery, edge effects have to be minimised. The use of minimally deleterious dicing techniques and proper surface-state passivation

is therefore imperative. Today, several designs of edgeless sensors are fabricated and examined. Depending on the way the edge is terminated, they can be categorised into two types: slim-edge and active-edge sensors.

Slim edges

Slim-edge structures are manufactured by dicing the sensor closer to the pixel matrix. As a consequence, the depletion zone extends to the edge (see Figure 2.12) and any charge generated at the edge will enter the space charge region, which is being referred to as charge injection. It is therefore crucial that the defect density at the edge is minimised. This is accomplished by avoiding and mitigating the negative effects of dicing. The literature reports on:

- Laser cutting and subsequent treatment of the edge's side-wall [67, 68]: both surface-state passivation by aging in air and defect removal by chemical treatment, e.g. etching the edge with an acid solution, show improvements of the performance of the sensor's active area.

- Deep reactive ion etching [69, 70]: this die-separation technique results in less surface damage than blade dicing and it can be easily implemented in a standard micro-electronics fabrication process.

- Current terminating structures [71–80]: narrow ring electrodes along the edge at the pixel side of the sensor. An important difference with regular guard rings is that they are grounded and hence do not gradually lower the potential towards the edge. They serve as a drain for the surface current that flows along the edges.

Recently, slim-edge p-type silicon sensor were realised by partial laser dicing and cleaving, followed by Al_2O_3 side-wall surface-state passivation [81]. The Al_2O_3 forms a negatively charged layer at the edge side-wall that pushes away free electrons and hence effectively passivates the edge. In fact, the Al_2O_3 not only passivates the edge's surface, but also shapes the electric field at the edge. This is similar to what active-edge sensors are based on.

Active edges

Active-edge sensors [82–85] are basically similar to slim-edge sensors, except that the electric field is actively terminated at the edge. Impurity atoms of the same doping type and concentration as the back side are implanted in the edges' side-walls, as a result of which they form an extension of the back electrode (see Figure 2.12). This configuration allows the pixel matrix to be as close as tens of micrometers from the edge. In spite of this major achievement, active-edge technology has its drawbacks:

- The fabrication process is complex. To be able to access the side-walls of the edge in order to do wafer-level doping a support wafer is required (this will be discussed in more detail in Chapters 4 and 5).

- The doped edge causes a distortion of the electric field in the edge region, which results in an anomalous response of the outer pixels. At the same time, the edge implant can cause a strong curvature of the junction at the edge, which could dramatically lower the break-down voltage of diode structures.

2.5 Summary

Crystalline semiconductor material is very suitable as a conversion layer for imaging detectors. They provide large signals and at the same time their conductivity is high enough to avoid high leakage currents. Nevertheless, the electrical integrity of the sensor material strongly depends on the homogeneity and purity of the crystal. Nowadays, detector-grade silicon wafers with a diameter of up to 300 mm can be produced, while the growth of compound semiconductor materials is much more complicated and much less under control. Typical maximum wafer diameters are 150 mm for gallium arsenide and 75 mm for cadmium telluride, which translates into even smaller pieces of homogeneous sensor material. As a consequence, the active area of current detectors using single-crystal cadmium telluride as sensor material is limited to approximately 10 cm^2. One way to realise a larger detection area is to tile multiple smaller detectors. This requires sensors that are homogeneously responding up to the edge, which means that edge effects have to be minimised. Minimally deleterious dicing as well as proper surface-state passivation is imperative. Two types of edgeless sensors are under study nowadays: slim-edge and active-edge sensors. Slim-edge sensors are fabricated by dicing the sensor closer to the pixel matrix, whereas active-edge sensor are characterised by the fact that the edge is doped. This implant actively terminates the electric field at the edge, which allows the pixel matrix to be as close as tens of micrometers from the edge.