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Öner, S.Z.

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Metal-insulator-semiconductor (MIS) junctions provide the charge separating properties of Schottky junctions while circumventing the direct and detrimental contact of the metal with the semiconductor. A passivating and tunnel dielectric is used as a separation layer to reduce carrier recombination and remove Fermi level pinning. When applied to solar cells, these junctions result in two main advantages over traditional p-n-junction solar cells: a highly simplified fabrication process and excellent passivation properties and hence high open-circuit voltages. However, one major drawback of MIS solar cells is that a continuous metal layer is needed to form a homogeneous junction at the surface of the silicon, which decreases the optical transmittance and hence short-circuit current density. The decrease of transmittance with increasing metal coverage can, however, be overcome by nanoscale structures. Nanowire networks exhibit precisely the properties that are required for MIS solar cells: closely spaced and conductive metal wires, to induce an inversion layer for homogeneous charge carrier extraction, and simultaneously a high optical transparency. We experimentally demonstrate the nanowire MIS concept by using it to make silicon solar cells with a measured energy conversion efficiency of 7% (~11% after correction). Furthermore, we introduce inverted nanopyramids integrated between the metal nanowire network, decreasing the reflectivity substantially from 36% to ~4%.
3 Metal-Insulator-Semiconductor Nanowire Network Solar Cells

3.1 Introduction

When a metal contacts a semiconductor, a carrier selective Schottky junction can be formed. The resulting conduction type inversion in the semiconductor depends on the metal and semiconductor work function difference. For example, when n-type silicon directly contacts a high work function metal (Au), the conductivity for electrons falls below the conductivity for holes close to the surface. This inversion of the majority carrier conduction type causes the carrier selective properties of Schottky junctions. However, as also shown in Chapter 2 the direct contact between metal and semiconductor can increase surface recombination due to metal-induced band gap states and dangling bonds and can even lead to Fermi level pinning at the semiconductor surface.\[84\] Metal-insulator-semiconductor (MIS) junctions circumvent those problems by separating the metal and semiconductor with a thin tunnel and passivating dielectric.\[85\] Furthermore, interface charges at the dielectric semiconductor interface can increase the magnitude of the conduction type inversion in the semiconductor.\[86\]

Because of their charge selective and passivating properties, MIS junctions were successfully used to make silicon solar cells starting in the 1970s.\[87, 88\] The MIS solar cell device architecture has two main advantages over traditional p-n junction cells: (1) highly simplified fabrication and (2) excellent passivation of the semiconductor even under the contact.\[87, 89\] For traditional solar cells, highly doped regions are required to induce the charge selectivity, with the disadvantage of increased Auger recombination. The reduced carrier recombination of MIS solar cells led to open-circuit voltage ($V_{oc}$) values of up to 655 mV, surpassing those of traditional p-n junction solar cells in early development stages.\[85\] More recently, the extraordinary potential of the MIS concept has emerged again, with recent record silicon solar cells employing a carrier selective, tunnel oxide passivated contact at the back side, which is conceptually identical to the MIS structure.\[89–91\] Furthermore, the MIS junction has emerged as one of the most successful interfaces in photocatalysis in recent years, where the metal induces charge separation, catalyzes the chemical reaction and protects the underlying semiconductor.\[92–95\]

One major difficulty in applying MIS contacts to the front of a solar cell is the increased reflection due to the required metal coverage for homogenous junction formation. Early generations of MIS solar cells utilized thin metal layers and hence exhibited low short-circuit current densities ($J_{sc}$), while advanced generations introduced widely spaced macroscopic contact fingers which reduced the reflection substantially and led to substantial performance improvements.\[96\] To form a homogenous junction under the whole surface, additional dielectric layers with a high fixed charge density were employed, which however were insufficient to induce junction properties similar to diffused junctions or continuous metal layers.\[96\] Therefore, a low reflectivity combined with a high quality homogenous MIS junction over the entire surface, which is especially needed for materials with short carrier diffusion lengths, remains to be a challenge for the MIS device architecture. The decrease of transmittance with increasing metal coverage of homogenous
MIS junctions can be overcome by nanoscale structures. Even though their electrical performance approaches those of continuous thin-films, engineered metal nanowire networks have been demonstrated to exhibit extraordinary transmission, where the transmission is larger than expected from geometric considerations.[97–102] Furthermore, nanowire networks can be fabricated on a large scale with roll-to-roll compatible processes, like nanoimprint lithography, or even using solution-synthesized metal nanowires.[103–106] Therefore, nanowire networks exhibit precisely the properties that are required for MIS solar cells: closely spaced and conductive metal wires, to induce a junction for homogenous carrier extraction, and simultaneously a high optical transparency.

Here, we demonstrate nanowire network based MIS silicon solar cells, by fabricating the nanowire networks on top of passivated silicon half cells using electron beam lithography. By choosing well passivated silicon as a base material, we are able to exclude any effects of short minority carrier diffusion lengths on our results. Our solar cells exhibit a measured conversion efficiency of 7%. After correcting for the influence of the small size of the active area on the $V_{oc}$ and the missing anti-reflection coating on the $J_{sc}$, we estimate that our MIS solar cells exhibit a corrected power conversion efficiency of $\sim 11\%$ with an effective $V_{oc}$ of 560 mV and estimated $J_{sc}$ of 33 mA/cm$^2$. We perform electron beam-induced current (EBIC) measurements to prove that nanowire networks can be used to form an MIS junction, which leads to homogenous charge carrier extraction. Band diagram simulations allow us to investigate the dependence of the conduction type inversion on the work function difference between the metal and the semiconductor and hence to explain the relatively low $V_{oc}$. Reflection measurements show that a high metal coverage of the surface with metal nanowire networks only slightly increases reflection compared to a flat silicon surface. Finally, we demonstrate a first step towards improved device performance by using the metal nanowire network not only as a transparent electrode and for the inversion layer formation, but also as an etch mask for surface texturing. We fabricate inverted nanopyramids integrated into the metal nanowire network. As a result, we are able to decrease the reflectivity substantially from 36% to $\sim 4\%$. We use external quantum efficiency (EQE) measurements to estimate the influence of the reduced reflection on the overall device performance and thereby point out a path towards MIS solar cells that exhibit both high $V_{oc}$ and $J_{sc}$ values.

3.2 Experiment

3.2.1 Fabrication

To isolate the effect of the metal nanowire network on the MIS solar cell performance, we use a state-of-the-art contact scheme for the back of the solar cell, which is employed in industrial silicon heterojunction (SHJ) solar cells (Figure 3.1(a)). It consists of 5 nm of intrinsic a-Si:H followed by 8 nm of n-type a-Si:H, 80 nm ITO and 300 nm Ag. Due to the importance of the tunnel and passivation layer, we rely
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Figure 3.1: Device schematic and SEM of nanowire network. (a) Device schematic, showing the different layers employed for the nanowire network MIS solar cell. Not to scale. (b) SEM images of the nanowire network with 100 nm nanowire width, 50 nm height and 1 µm pitch on top of the silicon half-cell, showing the high uniformity of the nanoscale pattern. A high-resolution SEM is shown as an inset.

on a high quality double layer for the front surface, consisting of 3 nm intrinsic hydrogenated amorphous silicon (a-Si:H), followed by 1 nm of Al₂O₃.[107] The intrinsic a-Si:H is grown by inductively coupled plasma chemical vapor deposition (ICP-CVD) and is used due to the excellent chemical passivation properties on the silicon surface. The Al₂O₃ layer is grown by atomic layer deposition (ALD) and is known for its high stability and insulating properties.[108] When used directly on silicon, ALD Al₂O₃ has been shown to exhibit a high fixed charge density, which can lead to a field effect passivation of the underlying surface.[109–111] Besides the additional passivation effect, the Al₂O₃ also serves as a capping layer to prevent the out diffusion of hydrogen from the intrinsic a-Si:H layer. The metal nanowire network is fabricated by electron beam lithography on small areas (2.4 - 4.5 mm²) and subsequent metal evaporation of Pd and Au. Pd was chosen due to the high work function to create a strong inversion layer, while Au was used because of lower optical losses than Pd. The low stability of Ag during subsequent processing precluded a possible usage of that metal. To integrate the inverted nanoparamid texturing in between the metal nanowire networks, the networks are fabricated on a silicon wafer, which is subsequently immersed in a KOH solution (further details in Supplemental Information).

3.3 Results

Figure 3.1(b) shows the fabricated Au-Pd nanowire network on top of the passivated substrate. The wires are 100 nm wide, 50 nm high (10 nm Pd/ 40 nm Au) and the pitch is 1 µm. The network is highly uniform and spans an area of 2.4 mm². Figure 3.2(a) shows the current density-voltage (J-V) traces of a masked nanowire network MIS solar cell under 1 sun illumination (green) and in the dark (red). The inset shows a schematic of the 2.4 mm² solar cell, which is created by fabricating a nanowire network (red) on top of a 2 cm² large substrate (blue). The silver back con-
3.3 Results

tact (grey), the contact probes (black) and the shadow mask (green) are indicated. The J-V curve in the dark shows a clear rectification. Under 1 sun illumination intensity, an open-circuit voltage ($V_{oc}$) of 423 mV, a short-circuit current density ($J_{sc}$) of 23 mA/cm$^2$ and a fill factor ($FF$) of 58% are obtained.

To account for the smaller size of the masked collection area (2.4 mm$^2$) compared to the substrate area (2 cm$^2$) we calculate the impact on the $V_{oc}$, with the main effect being the high contribution of the recombination current ($I_0$) originating from a larger area than the $J_{sc}$. As explained in detail in the SI, we use two different approaches to estimate the effective $V_{oc}$, both resulting in the same value of about 560 mV (see Figure 3.5-3.8). Finally, we estimate the current density with an antireflection (AR) ($n = 2$) coating with 10% residual reflectivity (simulated value), compared to the uncoated solar cell (36% measured reflectivity). Figure 3.2(b) shows a table with the measured and rescaled/estimated solar cell parameters, taking into account the aforementioned effects. As a result, the nanowire network MIS solar cell has an effective $V_{oc}$ of 560 mV, an estimated $J_{sc}$ of 33 mA/cm$^2$ and a $FF$ of 58%, resulting in an 11% energy conversion efficiency (after correction).

The results show that the metal nanowire network not only gives rise to charge carrier extraction, but also charge carrier separation inside the semiconductor, i.e. the metal nanowire network can potentially be used to replace the traditional contacts of an MIS solar cell. The small spacing of the metal networks makes our MIS concept applicable to materials with minority carrier diffusion lengths $\gtrsim 1$ µm, as is the case for many thin-film materials such as CIGS, CdTe, halide perovskites and GaAs (see also Figure 3.3).[112] However, our results also show that our obtained solar cell parameters, i.e. the $V_{oc}$, $J_{sc}$ and $FF$, are well below those of state of the

![Figure 3.2](image-url)

**Figure 3.2:** Device performance. (a) J-V trace of nanowire network MIS solar cells in the dark (red) and under 1 sun (AM1.5G) illumination intensity (green). The active area shown here has a size of 2.4 mm$^2$ on a 2 cm$^2$ substrate. The measurements are performed under masked conditions. The inset shows the experimental geometry, where the nanowire network (red) and the shadow mask (green) are used to define the cell area. (b) Table with the measured and rescaled/estimated solar cell parameters.
art silicon solar cells. Therefore, we conduct the following electrical and optical analyses to get insight into the device performance and to point out crucial steps towards improvements.

Figure 3.9 and 3.10 show band diagram simulations which have been performed to study the dependence of the conduction type inversion, and hence selectivity of the MIS contact, on the work function (WF) difference between the n-type silicon and the adjacent metal. The simulations show that high metal work functions (> 5 eV) can lead to strong conduction type inversion in the underlying silicon, the prerequisite for a high \( V_{oc} \). Conversely, any decrease of the effective metal WF will lead to a decrease in the \( V_{oc} \). After considering other possibilities, we conclude that the cause for the relatively low \( V_{oc} \), when compared to state-of-the-art silicon solar cells (>700 mV), can be the lowering of the Pd vacuum work function due to the presence of the dielectric Al\(_2\)O\(_3\). From developments in the field of complementary-metal-oxide-semiconductor (CMOS) transistors, it is known that Fermi level pinning to a charge neutrality level (CNL) in the dielectric can lower the effective work function of the metal.[113–115] Therefore, other dielectrics, e.g. SiO\(_2\), that cause much weaker Fermi level pinning to the CNL should be employed in future devices. However, when searching for alternatives the stability and passivation properties for ultrathin layers have to be kept in mind. For a detailed discussion see SI.

Besides the aforementioned reasons, the typically high costs associated with high WF metals (Ag, Au, Pd, Pt) and their potentially detrimental influence on the material quality (e.g. lifetime) have to be considered. Therefore, high WF oxides (e.g. MoO\(_x\)) are a promising alternative as an interfacial layer[28, 116, 117]. The same holds for layers of doped semiconductors, like n-type (and p-type) a-Si:H in high-efficiency silicon heterojunction (SHJ) solar cells.[10, 89, 118] However, as also

![Figure 3.3: Electron-beam-induced-current (EBIC) measurement.](image)

- **a** SEM image of a region of interest (ROI) of a similar sample to the one shown in Figure 3.2. Two residual metal flakes from the fabrication can be seen.
- **b** EBIC measurements, showing a uniform charge carrier separation and collection in the ROI due to the closely spaced metal nanowire network and the large carrier diffusion lengths in silicon. We note that the shadowed regions due to the metal nanowires are smaller for a sample under light illumination, because of efficient directional scattering by optical (plasmon) resonances.
3.3 Results

Our results show (see Figure 3.13) the stability and process compatibility, especially with nanostructuring have to be considered when employing such layers.\[119\]

Besides the degree of conduction type inversion, the simulations also show that the depth of the inversion layer extends to about 200 nm into the silicon, depending on the metal work function. Given the nanowire network pitch of 1 µm and assuming a constant radial extent of the inversion around the metal as an upper bound, a large fraction of the silicon square between the metal wires is inverted close to the surface. Electron-beam-induced-current (EBIC) measurements (Figure 3.3) show that this conduction type inversion, together with the large diffusion lengths in silicon lead to homogenous carrier collection.

As can be seen in Figure 3.2, the $J_{sc}$ of our solar cell reaches a value of 23 mA/cm$^2$. We ascribe the primary deviation from state-of-the-art silicon solar cells ($\sim 42$ mA/cm$^2$) to the high reflectivity of the uncoated and flat silicon substrate. Therefore, we measure the total reflectance of the completed devices using an integrating sphere setup. Then, we introduce a low reflectivity structure, consisting of nanopyramids integrated in between the nanowire network. We use EQE measurements to estimate the effect on the final device performance, as a first step towards improved $J_{sc}$ values for nanostructured MIS solar cells.

Figure 3.4(a) shows the measured reflection values of the nanowire network solar cell (blue), the network with integrated inverted nanopyramids (orange) and a bare polished silicon surface as reference (green). FDTD Simulations were used to obtain an estimate of the residual reflection when a standard anti-reflection coating (n=2) of 80 nm would be included on top of the flat nanowire network solar cell (violet). The average reflectivity ($\bar{R}$) in the wavelength range from 420 - 900 nm is also shown for the different structures. Figure 3.4(c) shows the measured external quantum efficiency (EQE, extracted charge carriers per incident photon) of the flat nanowire network solar cell (blue line). The curve shows relatively uniform quantum efficiency over the visible range. Taking into account the measured reflection and the simulated absorption in the metal, the internal quantum efficiency (IQE, extracted charge carriers per absorbed photon in the semiconductor) was determined (black line). For wavelengths below the band gap of silicon (1.1 eV) the IQE increases until it reaches unity in the range between 600 - 800 nm. For short wavelengths, the IQE drops to a value of $\sim 0.8$, indicating charge carrier recombination near the front surface. The effect of detrimental absorption in the metal can be seen for the IQE with the metal absorption (grey line). To estimate the effect of a standard SiN AR coating on the optical response of the solar cell, the EQE was calculated taking into account the simulated reflection of Figure 3.4(a) (violet dashed line).

The measurements and simulations in Figure 3.4(a) show that the nanowire network only adds a small amount of additional reflection, the value increases from 33% for a bare silicon surface to 36%. For this sample we measured a $J_{sc}$ of 23 mA/cm$^2$ (see Figure 3.4(a) and 3.4(c)). A standard 80 nm AR coating (n = 2) can reduce the reflection of the flat nanowire network silicon surface to $\sim 9\%$, which would result in a short-circuit current density of $\sim 33$ mA/cm$^2$ (see Figure 3.4(c)).
Figure 3.4: Reflection, EQE, IQE and inverted nanopyramids. (a) Reflection measurements (solid lines) of silicon reference wafer (green), a solar cell with a metal nanowire network (NWN) with a pitch of 1 µm and a nanowire width of 100 nm (blue) and a sample with integrated inverted nanopyramids between the metal nanowires (orange). Also shown are the simulated reflection values (dashed lines) of the flat metal network with 80 nm SiN coating for a wire width of 100 nm (violet) and the integrated inverted nanopyramid metal nanowire structure with 100 nm SiN coating on top of 50 nm wide wires (red). The average reflection values between 420 - 900 nm are listed next to the legend. (b) Scanning electron microscopy image of a metal nanowire network with integrated inverted nanopyramids. A high-resolution SEM is shown as an inset. (c) External quantum efficiency (EQE) of solar cell with metal nanowire network (blue). The IQE was determined by accounting for the reflection (blue line in (a)) and the simulated absorption of the metal network. The simulated reflection curves in (a) for the SiN coating (violet) and the integrated nanopyramid nanowire structure (red) were used to estimate the effect on the EQE of the final device. The respective short-circuit current densities are depicted next to the legend.

The measured $J_{sc}$ of 23 mA/cm$^2$ (see Figure 3.2(a) was obtained for a MIS solar cell with a bare nanowire network silicon surface with an average reflection of 36%. Therefore, the photocurrent density after subtracting the reflection losses amounts to 36 mA/cm$^2$ (grey curve in Figure 3.4(c), which shows that a large fraction of the photogenerated charges is collected. However, since it does not reach the maximum photocurrent density under 1 sun illumination for silicon ($\sim 44$ mA/cm$^2$), we conclude that other loss mechanisms must be present, which are discussed below.
Figure 3.11 shows the simulated reflection, transmission and absorption values for a metal nanowire network with the dimensions mentioned above on a flat silicon wafer. As can be seen, the averaged absorption amounts to ~10% in the 420 - 900 nm spectral range. Therefore, we conclude, that the short-circuit current density is partly lowered due to absorption in the metal by approximately 4 mA/cm$^2$ to the value of 36 mA/cm$^2$ (black curve in Figure 3.4(c)). A potentially detrimental influence of the tunnel junction, which could result in nonlinear current-voltage behavior, was ruled out by measurements of the $J_{sc}$ under different illumination intensities, which prove that the 1 nm Al$_2$O$_3$ has a negligible tunnel resistance under normal operation conditions (see Figure 3.12).[120] Previous research has shown that the insulator thickness for MIS type solar cells should not exceed 2 nm to limit the tunnel resistance.[87, 88] Another origin of the photocurrent loss can be related to fabrication-induced defect formation. After the fabrication of the metal nanowire networks we encounter strongly s-shaped I-V curves, which can be attributed to charge carrier extraction barriers at the contact-silicon interfaces.[77] We anneal our samples until the s-shape is completely removed. We ascribe the damage mostly to the electron beam exposure of the a-Si:H.[119] With increasing annealing temperatures, the $I_{sc}$ (and $FF$) of the solar cells is monotonically increasing. However, the $V_{oc}$ reaches its maximum at around 220 - 230 °C, after which it starts to decrease. Therefore, we chose the annealing temperature not to exceed 220 °C, recovering the maximum $V_{oc}$, while being aware of the non-optimized $I_{sc}$ (and $FF$) values, due to residual fabrication induced defects. For further explanation, see the Figure 3.13. The IQE (black curve) in Figure 3.4(c) shows a decrease in IQE for short wavelength until it reaches ~0.8. This supports our assumption as light in the short wavelengths range is absorbed close to the surface, where the fabrication induced defects must be located. Therefore, the annealing behavior and the absorption in the metal nanowire network discussed above can explain the main difference between the $J_{sc}$ of our solar cells (36 mA/cm$^2$, after reflection) and a $J_{sc}$ of 42 mA/cm$^2$, which is reached by highly efficient silicon solar cells. We note that other losses, such as parasitic absorption in the thin a-Si:H layer, are likely to be present.[121]

As a first step towards improved $J_{sc}$ values for nanostructured MIS solar cells, we fabricate inverted nanopyramids integrated in between the metal nanowire network. Bare inverted nanopyramids with optimized pitch and additional AR coating have shown outstanding optical performance.[122, 123] Furthermore, etch resistant metals, such as the ones employed for our metal nanowire network, are frequently used as masking layers in micro-and nanofabrication.[124, 125] Figure 3.4(b) shows a scanning electron microscopy (SEM) image (magnified in the inset) of the fabricated inverted nanopyramid nanowire network structure. The measured reflection of the network with inverted pyramids (Figure 3.4(a), solid yellow line) shows clear resonant features due to the diffraction modes created by the effective grating. The average reflectivity of 19% proves the strong decrease in reflection compared to the flat nanowire network surface. By simulating an additional AR coating of 100 nm on top of the nanopyramid structure and a nanowire width of
50 nm instead of 100 nm (Figure 3.4(a), dashed red line) we show that the residual reflection can be even further reduced to 4%, which is well below the optimized AR coating for a flat silicon nanowire network surface (9%) (solid violet line). Figure 3.4(c) shows the effect of the integrated nanopyramid texturing on the EQE (red dashed curve), which results in a $J_{sc}$ of $\sim 35$ mA/cm$^2$. We stress that a further decrease in reflection with optimized dimensions, e.g. AR coating thickness and wire thickness, can be expected. However, the optimization of the non-trivial optical response, as well as the integration into the solar cell fabrication process of the metal nanowire network with integrated nanopyramids is beyond the scope of this report and focus of ongoing research.

3.4 Conclusions

We successfully apply metal nanowire networks to the MIS solar cell scheme. After correcting for the influence of the small size of the active area on the $V_{oc}$ and the missing anti-reflection coating, our MIS solar cells exhibit a corrected power conversion efficiency of $\sim 11\%$ with an effective $V_{oc}$ of 560 mV and estimated $J_{sc}$ of 33 mA/cm$^2$. We use EBIC measurements to show that the metal nanowire network homogenously extracts charge carriers via an inversion layer in the underlying silicon. Band diagram simulations allow us to investigate the dependence of the conduction type inversion on the work function difference between the metal and the semiconductor and indicate the occurrence of Fermi level pinning at a charge neutrality level at the metal dielectric interface. Reflection measurements show that a high metal coverage of the surface with metal nanowire networks only adds 3% of additional reflection compared to a flat silicon surface.

Finally, we demonstrate a first step towards improved device performance by using the metal nanowire network not only as a transparent electrode and for the inversion layer formation, but also as an etch mask for surface texturing. We fabricate inverted nanopyramids integrated into the metal nanowire network. This way we are able to decrease the reflectivity substantially from 36% to $\sim 4\%$. We use external quantum efficiency (EQE) measurements to estimate the influence of the reduced reflection on the overall device performance and thereby point out a path towards MIS solar cells that exhibit both high $V_{oc}$ and $J_{sc}$ values. Furthermore, our work shows potential for the MIS concept to be used to directly contact well passivated, intrinsic semiconducting layers, which naturally show higher carrier lifetimes and mobilities and are therefore preferable for high efficiency solar cells. Finally, our results are not limited to silicon, but can be applied to many thin-film materials with small charge carrier diffusion lengths where the difficulty of doping makes carrier selective contact formation more challenging.
3.5 Supplemental information

3.5.1 Fabrication details

To isolate the effect of the metal nanowire network on the MIS solar cell performance, we are using a state-of-the-art contact scheme for the back of the solar cell, which is employed in industrial solar cells (see Figure 3.1). This half cell consists of a double side polished float zone silicon base wafer with low n-type doping (3 Ohmcm), followed by different layers which create the back contact; a thin-film of intrinsic hydrogenated amorphous silicon (a-Si:H) (5 nm) followed by a layer of highly doped n-type a-Si:H (8 nm) are grown on the silicon wafer by plasma enhanced chemical vapor deposition (PECVD, Roth & Rau). The n-type a-Si:H is contacted via a sputtered indium tin oxide (ITO) layer (80 nm), followed by a sputtered silver layer (300 nm) as metal contact (Roth & Rau AK tool system).

The passivating and insulating layer, which is grown on the front surface after a short HF treatment (45 s in 1%), consists of 3 nm intrinsic a-Si:H followed by 1 nm of Al$_2$O$_3$.[107] The a-Si:H is grown by inductively coupled plasma chemical vapor deposition (ICP-CVD, PlasmaLab System 100, Oxford Instruments) and is used due to the excellent chemical passivation properties on the silicon surface. An argon and silane flow of 20 sccm, a temperature of 50 °C and a power of 400 W at a pressure of 10 mTorr were used for 24 s (~ 3 nm thickness). The Al$_2$O$_3$ layer (9 cycles with a total nominal thickness of ~ 1 nm) is grown by atomic layer deposition (ALD) (OpAL, Oxford Instruments) at 190 °C with trimethylaluminum (TMA) and O$_2$ plasma. Al$_2$O$_3$ is known for its high stability and insulating properties. When used directly on silicon, ALD Al$_2$O$_3$ has been shown to exhibit a high fixed charge density, which can lead to a field effect passivation of the underlying surface.[108–111] Subsequently, the samples were exposed to N$_2$ atmosphere in a rapid thermal annealing oven at 190°C for 30 min.

The passivated and back contacted half cells were fabricated on 4 inch wafers, which were subsequently cut into about 2-3 cm$^2$ small pieces to allow the optimization of the following fabrication steps.

The square metal network (nanowire width ~ 100 nm, network pitch ~ 1-2 μm) is fabricated by electron beam lithography (EBL) on small areas (2.4 - 4.5 mm$^2$) on ~ 2 cm$^2$ substrates. EBL resist ZEP 520 A (Zeonrex Electronic Chemicals) is used in a 2:1 mixture with anisole and spun (1000 rpm for 40 s) to achieve a resist thickness of ~ 200 nm. Afterwards, the substrates are baked at 180 °C for 5 min. The resist is exposed with 30 kV beam acceleration at a dose of 400 μC/cm$^2$ (10 μm aperture) in a fixed beam-moving stage modus (FBMS), with a predefined square nanowire network structure with pitches of 1 μm and 2 μm. After developing in penty lactate for 1 min the samples are rinsed for 15 s in a 9:1 mixture of methyl isobutyl ketone (MIBK) and isopropanol (IPA) and additionally for 15 s in pure IPA.

The samples are blow-dried with nitrogen and transferred to the vacuum chamber of an electron beam evaporator. At a pressure of ~ 5×10$^{-7}$ mbar, first a 10 nm thin layer of palladium, followed by a 40 nm thin layer of gold are evaporated at a
rate of 0.2 - 0.5 Å/s from water-cooled copper and tungsten crucibles, respectively. The Pd and the Au pellets are of at least 99.95% purity. This double structure is used because of the higher work function (WF) of Pd (5.2 - 5.6 eV) than Au (5.1 - 5.5 eV), which allows a stronger inversion in the underlying silicon, and the lower optical losses of Au compared to Pd.

After the evaporation, the samples are immersed in warm acetone (50 °C) to dissolve the EBL resist and this way lift-off the redundant metal film, leaving behind the desired square metal nanowire network structure. Metal pads for later contacting purposes are placed on two sides of the square network with conventional UV lithography and subsequent metal evaporation, using a 100 nm, opaque Au layer.

Electron beam (e-beam) and intense UV light exposure is known to cause damage in a-Si:H. Therefore, the samples are subsequently transferred into a vacuum oven and annealed for 60 min at a pressure of 5x10^{-5} mbar and a temperature of 220 °C to reverse the majority of the damage (see Figure 3.13).

The integrated inverted nanopyramids in between the metal nanowire network were fabricated by first fabricating the metal nanowire network on a simple silicon wafer and subsequently immersing the sample into KOH etching solution (30%) for 2 min. at a temperature of 20 °C. The metal (Pd/Au) nanowire network acts as an etching mask for the KOH solution and allows therefore the crystal plane selective dissolution of silicon, with the (111) crystal plane having the slowest etch rate.

### 3.5.2 Electrical and optical characterization

The J-V traces of the fabricated solar cells are measured under a solar simulator (Oriel SOL2 94062A (6X6) Class ABA, Newport) with the AM1.5G spectrum at 1 sun (100 mW/cm²) illumination intensity, under masked conditions and at a temperature of 50 °C. The lamp intensity of the solar simulator is adjusted with a silicon reference cell. The right masking conditions are a crucial step for our solar cells, as the network only covers a small part (2 - 4.5 mm²) of the passivated silicon half cells (2-3 cm² small substrates) (see Figure 3.5). Electrical probes are used to contact the front pad of the nanowire network and the back contact of the whole substrate with a source measure unit (Agilent B2910). The voltage is scanned with a positive and negative scan rate between -1V and 1V in 2001 steps while the current is being measured. No pronounced hysteresis or instability could be detected during the course of the measurements.

A lifetime of 1 ms was measured on the back contacted (w/o ITO) and front passivated silicon wafers before the nanowire network fabrication with a Sinton WCT-120TS lifetime tester.

The reflection measurements are performed using an integrating sphere setup. A supercontinuum white light source (Fianium) is used to illuminate the solar cells. The unpolarized light is weakly focused on the back plane of the sphere (4 inch Labsphere) to ensure near to normal incidence. A 105 μm core fiber is used to collect the reflected light and send it to a spectrometer, consisting of a spectrograph (Spectraphot Pro 2300i ) and a Si CCD array (PIXIS 400 CCD, cooled to -70 °C). The
measurements cover the 420 - 970 nm spectral range, and a 400 ms integration time with 50 accumulations were used.

### 3.5.3 Simulations

The band diagram simulations are performed with the software package AFORS-HET.[126] The simulated structure consists of an n-type Si wafer with a base doping of $1.6 \times 10^{15}$ cm$^{-3}$, a 3 nm intrinsic a-Si:H layer, a 1 nm Al$_2$O$_3$ layer and a metal contact which is simulated by having a fixed work function as boundary condition. Fixed charge is placed at the a-Si:H/Al$_2$O$_3$ interface. For the material properties, the default simulation values provided by AFORS-HET are used. Simulations are performed in the dark.

The finite difference time domain (FDTD) simulations are performed with the software package Lumerical to obtain the reflection values for the 80 nm silicon nitride coated (n = 2) network with and without integrated inverted nanopyramids. The network has a pitch of 1 µm, a nanowire width of 100 nm (50 nm for red data in Fig. 3.4) and a thickness of 50 nm, with 40 nm of Au (top) and 10 nm Pd (bottom). A plane wave ($\lambda = 400 - 1100$ nm) under normal incidence and a power monitor, positioned above the nanowire network, are used to determine the reflectance. A perfectly matched layer as boundary condition in vertical direction is used to prevent scattering artifacts from the edges of the simulation box, while periodic boundary conditions are used for the in-plane dimensions to simulate an infinite network. The mesh size was 2 nm and the optical constants for Au, Pd and Si are taken from Palik.

### 3.5.4 Influence of active area size

In the following, we investigate the effect of the small size (2.4 - 4.5 mm$^2$) of the illuminated area on the open-circuit voltage. The illuminated area equals the area

![Figure 3.5: Influence of masking condition.](image)

(a), (b) The measurements under illumination are done with a mask (green), which covers the areas of the passivated and back contacted silicon substrate (blue). The mask has an opening in the middle, which allows illumination of the area with the fabricated metal nanowire network (red). (c) The measured $V_{oc}$ is strongly affected by the relatively larger contribution of $I_0$ compared to $I_L$. Therefore, the effect is investigated and an effective $V_{oc}$ derived, which allows the estimation of the solar cell performance, for which the substrate has the same size as the active area, as depicted here.
of the nanowire network, which has been limited in size due to the use of e-beam lithography. Taking into account that $J_0$ stems from a much larger region than the photocurrent, we are able to estimate the open-circuit voltage for a 1 cm$^2$ sample. This way we are able to evaluate and compare our results with regard to other solar cell device architectures.

We use two approaches, based on two separate sets of measurements, that both yield the same result for the estimated $V_{oc}$. The first approach investigates the scaling behavior of the recombination parameter $J_0$ with different sample sizes.

The second approach studies the variation of the $V_{oc}$ for two different measurements; under masked and under unmasked conditions. This second approach makes use of the fact that the $V_{oc}$ can be related to the carrier concentration inside the solar cell (implied $V_{oc}$).[19]

Because we employ high-purity monocrystalline FZ-silicon wafers we attribute the main contribution to $J_0$ to stem from recombination active surface sites. This surface recombination originates mostly from a larger area than the illuminated one. It is facilitated via diffusion of carriers to unilluminated regions and further to respective recombination sites. The diffusion is therefore taking place because of the difference in the carrier concentrations between the illuminated and the dark regions and between the recombination inactive bulk and recombination active surface.

**Scaling behavior of $J_0$ with active area size**

We compare three samples (S1-S3) that are fabricated in the exact same way but with different sizes of the metal nanowire network (2.4 - 4.5 mm$^2$). The short-circuit current density for 1 sun illumination is approximately the same for all the fabricated samples which strongly supports the reproducibility of our fabrication scheme.

$J_0$ mainly originates from surface recombination. However, the exact size of the surface area which causes $J_0$ is unknown. Under illumination, the diffusion

![Figure 3.6: Origin of large recombination current.](image)

(a) The main contribution to $J_0$ is originating from surface recombination, as derived and described in the text. (b) The illuminated area $A_L$ is much smaller than the area $A_S$, which significantly contributes to the recombination current density $J_0$. 

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of photo-generated charge carriers to recombination active surface sites has to be taken into account and hence forbids any simple estimation of the contribution of any single dimension or region (e.g. the whole substrate area). Nonetheless, by using three samples, that have been fabricated under the exact same conditions, but are of different size, and investigating the scaling behavior of the recombination current density $J_0$, we are able to estimate the value of $J_0$ for a standardized sample size of 1 cm$^2$.

The ideal diode equation results in the well-known $V_{oc}$ equation:

$$V_{oc} = \frac{n \times k_B T}{q} \times \ln \left( \frac{J_L}{J_0} + 1 \right) \sim \frac{n \times k_B T}{q} \times \ln \left( \frac{J_L}{J_0} \right)$$  \hspace{1cm} (3.1)

with the ideality factor $n$, the Boltzmann constant $K$, temperature $T$, the elementary charge $q$, the photocurrent density $J_L$ and the recombination current density $J_0$.

In the following, we assume an ideality factor of $n = 1$, but this assumption has no influence of the scaling of $J_0$. Using the above equation, we calculate the recombination parameter $J_0$ for the three samples under illumination. The temperature during the measurements was $\sim 50 \, ^\circ C$ (323 K) and the respective measured $V_{oc}$ and $J_{sc}$ values are listed in Table 3.1:

$$J_0 = \exp \left( -\frac{V_{oc}}{27.8 \, mV} \times J_L \right)$$  \hspace{1cm} (3.2)

$J_0^{S_1} = 6.60 \times 10^{-9} A/cm^2$, $J_0^{S_2} = 2.90 \times 10^{-9} A/cm^2$, $J_0^{S_3} = 1.68 \times 10^{-9} A/cm^2$.

In general, $J^{tot}_0$ can be expressed as the sum of the different recombination processes:[127]

$$J^{tot}_0 = J^{surf}_0 + J^{SRH}_0 + J^{Aug}_0 + J^{Rad}_0.$$  \hspace{1cm} (3.3)

$J^{surf}_0$ stems from surface recombination, $J^{SRH}_0$ from Shockley-Read-Hall (SRH) recombination, $J^{Aug}_0$ from Auger recombination and $J^{Rad}_0$ from radiative/ band-to-band recombination. Often, $J^{tot}_0$ is also separated according to the different regions in the solar cell from which the respective $J_0$ originates (e.g. for a n$^-$-emitter). As

<table>
<thead>
<tr>
<th>Sample</th>
<th>Area [mm$^2$]</th>
<th>$V_{oc}$ [mV]</th>
<th>$J_{sc}$ [mA/cm$^2$]</th>
<th>$J_0$ [A/cm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>2.4</td>
<td>419 (M)</td>
<td>23.2 (M)</td>
<td>660x10$^{-11}$ (C)</td>
</tr>
<tr>
<td>S2</td>
<td>3</td>
<td>439 (M)</td>
<td>21.0 (M)</td>
<td>290x10$^{-11}$ (C)</td>
</tr>
<tr>
<td>S3</td>
<td>4.5</td>
<td>457 (M)</td>
<td>23.3 (M)</td>
<td>168x10$^{-11}$ (C)</td>
</tr>
<tr>
<td>$S_{a-1}$</td>
<td>100</td>
<td>562 (C)</td>
<td>23.2 (E)</td>
<td>3.97x10$^{-11}$ (F)</td>
</tr>
</tbody>
</table>

Table 3.1: Solar cell parameters for differently sized samples. Measured (M), calculated (C), estimated (E) and fitted (F) solar cell parameters of the small area samples S1-S3 and the estimated 1 cm$^2$ sample $S_{a-1}$.
mentioned above, we expect the main contributor to be $J^\text{Surf}_0$ due to the absence of highly doped regions and the high crystal quality of the FZ-silicon base wafer.

For our small samples we expect approximately a $1/A_i$ dependence for the $J_0$, especially with increasing area size up to $1 \text{ cm}^2$. The total recombination current can be approximated as a constant that originates from a much larger area (for surface recombination) or volume (for SRH and Auger): 

$$J^\text{Si}_0(A_i) = J_0^{\text{Tot}}.$$  \hfill (3.4)

For increasing area size, but with $A_i < 1 \text{ cm}^2$, $J_0$ approaches more accurately a value that represents the recombination originating from a $1 \text{ cm}^2$ sample. However, for the measured samples we expect a deviation from the $1/A$ dependency, due to the nature of our samples. As we show in Figure 3.13, we observe electron beam-induced damage in the top 3 nm a-Si:H layer which can mostly be removed with a post fabrication anneal. However, as we discuss below, we are not able to remove all the induced damage. We choose an annealing temperature that is optimized with regard to the $V_{oc}$, but we cannot prove that this maximum $V_{oc}$ is completely unaffected by the damage. As a result, we expect a slightly higher $J_0$ for the fabricated samples, than a simple $1/A$ dependency would suggest. However, even for those samples the major $J_0$ contribution will stem from a much larger area than the illuminated one, unrelated to the electron beam-induced degradation.

Because of those reasons, we use a least squares fit method, to fit an equation of the following form to our calculated $J_0$ values:

$$f(x) = \frac{p}{x + q}$$  \hfill (3.5)
As shown in Fig. 3.7, we obtain good agreement with $p = 3.90 \times 10^{-09}$ and $q = -1.85:

$$J_0^{S_a} \sim \frac{3.90 \times 10^{-9}}{A_x - 1.85} A/cm^2$$

(3.6)

Therefore, we can estimate the recombination parameter $J_0^{S_a}$ for a 1 cm$^2$ large sample:

$$J_0^{S_a} = 3.97 \times 10^{-11} A/cm^2$$

(3.7)

Finally, we can calculate the $V_{oc}$ of the 1 cm$^2$ sample $S_a$, assuming a short-circuit current density as observed for samples S1 and S3, i.e. $\sim 23.2 mA/cm^2$. As discussed above, setting the ideality factor to $n = 1$ does not influence our result, as the estimated $J_0^{S_a}$ would have been higher for $2 > n > 1$.

$$V_{oc}^{S_a} \sim n \times 27.8 mV \times ln \left( \frac{J_L^{S_a}}{J_0^{S_a}} \right)$$

(3.8)

$$V_{oc}^{S_a} \sim 562 mV \ (n = 1, \ J_L^{S_a} = J_L^{S_1})$$

(3.9)

**Influence of masking conditions on carrier concentrations**

The second approach makes use of the fact, that the $V_{oc}$ is related to the carrier concentrations:[19]

$$V_{oc}^{imp} = k_T \times ln \left( \frac{(N_A + \Delta n)\Delta n}{n_i^2} \right)$$

(3.10)

$N_A$ is the doping concentration, $\Delta n$ is the excess and $n_i$ the intrinsic carrier concentration. $V_{oc}^{imp}$ is the implied open-circuit voltage, because it can be seen as the $V_{oc}$ that is implied by the carrier concentrations inside the semiconductor. For the actual $V_{oc}$ the energy levels of the contacts for the charge carrier extraction have to be considered, as well. By comparing measurements under illumination of a masked and an unmasked sample we can show that the carrier concentration for the masked sample is the limiting case. The energy levels of the contacts, determined by the metal WF for the (MIS) hole contact and the a-Si:H n-type doping for the electron contact, allow for a substantially higher $V_{oc}$.

As shown in Figure 3.8, the lateral diffusive currents lead to a decrease in the carrier concentrations in the small illuminated region. This decrease directly results in a decrease in the quasi-Fermi level splitting, i.e. the $V_{oc}^{imp}$. In other words, the carrier concentration is reduced compared to a case of complete substrate illumination. For the latter, only gradients in the carrier concentrations due to the surface recombination exist. However, the interpretation of an unmasked measurement for which the complete substrate is illuminated has to be done with caution.

First of all, only a small part of the area that is illuminated is also patterned with the nanowire network. The optical properties of the flat metal nanowire network on top of silicon are very similar to a flat bare silicon substrate, i.e. 36 vs. 33%
Figure 3.8: Schematic band diagram with lateral diffusion. Differences in carrier concentrations between the illuminated and the dark regions inside the bulk n-type wafer lead to gradients in the quasi-Fermi levels. Those in turn result in diffusive transport (red arrows) away from the illuminated region. The result is a lower implied $V_{oc}$.

reflection, and 10 % additional absorption, as shown in Figure 3.4. However, because of the logarithmic dependence of the $V_{oc}$ on the $I_{sc}$, the overestimation can be neglected. Therefore, the $V_{oc}$-loss due to lateral diffusion, $\Delta V_{oc}^{diff}$, is given by:

$$\Delta V_{oc}^{diff} = V_{oc}^{S_{1,nomask}} - V_{oc}^{S_{1,mask}} - V_{oc}^{S_{1,optical}} \approx 100 \text{mV}$$  (3.11)

$\Delta V_{oc}^{S_{1,optical}}$ is the $V_{oc}$-overestimation due to the lower reflection of the bare silicon surface and the absence of metal absorption. However, as we argued above, $V_{oc}^{S_{1,optical}} \approx 0 \text{mV}$. $V_{oc}^{S_{1,nomask}}$ and $V_{oc}^{S_{1,mask}}$ are the open-circuit voltages of the unmasked and masked samples, respectively.

Furthermore, the $I_{sc}$ of the unmasked sample is substantially higher than for the masked sample, especially for high purity silicon with its large minority carrier diffusion lengths. However, it does not reach the $I_{sc}$ values predicted for a 1 cm$^2$ sample, i.e. 23 mA. For our measurement the unmasked $I_{sc}$ is about 10 times higher than the masked one, i.e. 5.58 mA vs. 0.557 mA, as shown in Table 3.2. Therefore, we can estimate the area to be roughly 10 times larger than the 2.4 mm$^2$ small sample (neglecting the slightly different optical properties). Furthermore, the recombination current $I_0$ for a 24 mm$^2$ area is close to the value for a 100 mm$^2$ area (see also the extensive discussion above). Hence, we can estimate the additional gain in $V_{oc}$
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Table 3.2: Measured solar cell parameters with and without mask. Measured solar cell parameters of the small area sample S1 with and without a shadow mask. Calculated (C) and estimated (E) parameters for the 1 cm$^2$ sample $S_a$ due to an increase of $I_{sc}$ to 23 mA, with the term $\Delta V_{oc}^{light}$.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Area [mm$^2$]</th>
<th>$V_{oc}$ [mV]</th>
<th>$I_{sc}$ [mA]</th>
<th>$I_0$ Factor</th>
<th>$I_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1^m$</td>
<td>2.4</td>
<td>419</td>
<td>0.557</td>
<td>–</td>
<td>$I_0^{sunm}$</td>
</tr>
<tr>
<td>(masked)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$S_{sunm}$</td>
<td>~ 24</td>
<td>519</td>
<td>5.580</td>
<td>1</td>
<td>$I_0^{sunm}$</td>
</tr>
<tr>
<td>(unmasked)</td>
<td>(unknown)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$S_a$</td>
<td>100</td>
<td>559 (C)</td>
<td>23.3 (E)</td>
<td>4.17</td>
<td>$I_0^{S_a}$</td>
</tr>
</tbody>
</table>

for a 100 mm$^2$ sample due to an increase of $I_{sc}$ to 23 mA, with the term $\Delta V_{oc}^{light}$.

$\Delta V_{oc}^{light} = 27.8 \times \ln(4.17) \approx 40 \text{ mV}$  \hspace{1cm} (3.12)

We note, that this approximation leads to a conservative estimate of the additional $V_{oc}$-gain because we use an $I_0$ that stems from a 100 mm$^2$ sized sample. Another deviation is expected due to the less efficient carrier extraction in the case of the unmasked sample which heavily impacts the resistance and hence fill factor of the unmasked solar cells. The current of 5.58 mA of the unmasked sample is separated and collected with the same inversion layer and metal nanowire network than the 0.557 mA of the masked sample. Nonetheless, we can estimate the $V_{oc}$ for a 1 cm$^2$ sample:

$\Delta V_{oc}^{S_{a-2}} = V_{oc}^{S_{a-2}} + \Delta V_{oc}^{light} \left( I_0^{S_{a-2}} \sim I_0^{sunm} \right) + \Delta V_{oc}^{diff} = 559 \text{ mV}$  \hspace{1cm} (3.13)

Comparing the scaling behavior of the $J_0$ and the variation of the $V_{oc}$ for different masking conditions shows close agreement for the $V_{oc}$ of a 1 cm$^2$ sample:

$V_{oc}^{S_{a-1}} = 559 \text{ mV}$ \hspace{1cm} $V_{oc}^{S_{a-2}} = 562 \text{ mV}$  \hspace{1cm} (3.14)

3.5.5 Band diagram simulations

Influence of work function

Figure 3.9 shows the results of band diagram simulations, which are performed to investigate the influence of different metal work functions (WF) on the inversion of the n-type silicon. For the chosen WFs between 4.6 - 5.6 eV the conduction bands ($E_C$) and the valence bands ($E_V$) are plotted. All the Fermi levels ($E_F$) are set to 0 eV for clarity. The metal next to the adjacent Al$_2$O$_3$ is not shown. As can be seen, the WF of the metal determines the extent of the conduction type inversion in the semiconductor. N-type silicon has a WF of around 4.2 eV, hence employing metals with higher WFs reduces the free electron concentration in the n-type silicon, even leading to strong conduction type inversion in the extreme case. For comparison,
Figure 3.9: Band diagram simulations for the metal work function influence.

Band diagram simulations showing the influence of the metal work function for the conduction type inversion in silicon. The conduction bands ($E_C$) are plotted in the upper half ($E>0$ eV) and the valence bands ($E_V$) in the lower half of the figure ($E<0$ eV). For a better overview all the Fermi levels ($E_F$) are set to 0 eV.

Silicon that is strongly p-type doped ($p^+$) has a WF of around 5.3 eV. The simulations show that for WFs between 4.6 - 5.2 eV, an increase in the WF leads to increased inversion. Above ~ 5.2 eV on the other hand, the additional inversion with increasing metal WF becomes less pronounced. Besides the logarithmic dependence of the Fermi level position, part of this decreasing sensitivity of the inversion with increasing WF can be ascribed to the intrinsic (low conductivity) a-Si:H. Between 5.2 - 5.6 eV the initial energy difference of the conduction bands (red, violet and blue lines) at the metal - a-Si:H interface falls off over the intrinsic a-Si:H.

In the simulations shown here, no additional fixed charge density ($Q_f$) of the Al$_2$O$_3$ at the metal - a-Si:H interface is assumed. As shown in Figure 3.10, and discussed in detail below, only an additional fixed charge density with very high (negative) $Q_f$ values of around $10^{13}$ cm$^{-2}$ has a substantial effect for high WF metals. For low WF metals (<5 eV) $Q_f$ values above $10^{12}$ cm$^{-2}$ can already substantially improve the inversion.

**Influence of fixed charged density**

Al$_2$O$_3$ is known to exhibit a fixed charge density at a Al$_2$O$_3$-silicon interface, which can lead to electrical passivation of the interface, by repelling minority carriers with the same polarity of the surface charge. This so called field-effect passivation is being used in solar cells to increase the lifetime of the minority carriers by preventing their diffusion towards recombination active surface/interface sides. For the tunnel and passivation layer employed in this work, consisting of a 1 nm Al$_2$O$_3$
3.5 Supplemental information

![Band diagram simulations for the influence of a fixed charged density](image)

**Figure 3.10: Band diagram simulations for the influence of a fixed charged density.** Band diagram simulations showing the influence of a fixed charge density in the Al\(_2\)O\(_3\) at a given metal work function (WF) for the conduction type inversion in the silicon. The conduction bands (\(E_C\)), the valence bands (\(E_V\)) and the Fermi levels (\(E_F\)) are indicated, as well as the boundary regions in between the different employed layers. The metal, positioned left to the Al\(_2\)O\(_3\), is not shown. (a) Conduction type inversion for a metal work function of 4.6 eV and a fixed charge density \(Q_f\) between 0 cm\(^{-2}\) and 10\(^{13}\) cm\(^{-2}\). (b) The same as in (a), but with a metal work function of 5 eV.

and a 3 nm a-Si:H layer, the occurrence of a fixed charge density is being debated at the moment. Therefore, we performed band diagram simulations to investigate the effect of a potential fixed charge density on the magnitude of the inversion layer. In principle, a fixed charge density could lead to a stronger inversion in MIS type solar cells than given by the difference in work function between the metal and the adjacent semiconductor. Figure 3.10 shows the magnitude of the conduction type inversion for a metal work function of 4.6 eV (3.10(a)) and 5 eV (3.10(b)) in dependence of a fixed charge density at the Al\(_2\)O\(_3/\)a-Si:H interface. The interface charge density \(Q_f\) changes between 0 cm\(^{-2}\) and 10\(^{13}\) cm\(^{-2}\). As can be seen in Figure 3.10(a), for a metal work function of 4.6 eV the additional fixed charge density can have a very strong effect on the magnitude of the inversion layer. However, as can be seen in Figure 3.10(b) for a higher metal work function of 5 eV, even without a fixed charge density the inversion already reaches the same magnitude than for a work function of 4.6 and a very high fixed charge density of 10\(^{13}\) cm\(^{-2}\). Furthermore, any additional fixed charge density only has a relatively smaller effect on the conduction type inversion for a metal work function of 5 eV. This can be understood by the logarithmic dependence of the Fermi level position in the band gap with carrier concentration.

We conclude, that additional (negative) fixed charge density can lead to a stronger conduction type inversion (and hence higher \(V_{oc}\)), however the difference between the metal and the semiconductor work function has a more pronounced effect.
**Explanation of the low open-circuit voltage**

The simulations show that high metal work functions (> 5 eV) can lead to strong conduction type inversion in the underlying silicon, the prerequisite for a high $V_{oc}$. Conversely, any decrease of the effective metal WF will lead to a decrease in the $V_{oc}$. When corrected for the small illuminated area of our cells compared to the large substrate, the calculated effective $V_{oc}$ is 560 mV. The WF of high purity Pd is reported to be in the range of 5.2 - 5.6 eV, with the exact value being crystal facet dependent.[128] Given our surface passivation scheme and the high purity of the FZ-silicon wafer, even a slightly lower work function of Pd due to trace amounts of impurities seems insufficient to explain our results (see Figure 3.9).

A cause for the relatively low $V_{oc}$, when compared to state-of-the-art silicon solar cells (>700 mV), can be the lowering of the Pd vacuum work function due to the presence of the dielectric Al$_2$O$_3$.[113] From developments in the field of complementary-metal-oxide-semiconductor (CMOS) transistors, it is known that Fermi level pinning to a charge neutrality level (CNL) in the dielectric can lower the effective work function of the metal.[113–115] As a result, the effective WF of Pd is lowered to the range of 4.6 - 4.9 eV by the dielectric Al$_2$O$_3$, which is well below the reference WF of highly doped p-type silicon (~5.2 eV). Therefore, other dielectrics, e.g. SiO$_2$, that cause much weaker Fermi level pinning to the CNL should be employed in future devices. However, when searching for alternatives the stability and passivation properties for ultrathin layers of 1-2 nm have to be kept in mind.

We note that a strong inversion in the underlying silicon is not the only factor to consider for high open-circuit voltages in MIS silicon solar cells. To exclude fabrication induced material degradation as a major cause for the low $V_{oc}$, lifetime measurements after each fabrication step would be highly desirable. Unfortunately, the specific process sequence (e.g. the initial fabrication of the metalized backside) does not allow to track the lifetime with the Sinton lifetime tester. Besides the observed electron beam-induced damage of the a-Si:H (Figure 3.13), other steps known to negatively impact the passivation were avoided.

Furthermore, the selectivity of the contacts will fundamentally determine the degree to which the implied open-circuit voltage ($V_{oc}^{imp}$) can be translated to the measured $V_{oc}$.[19, 90, 129, 130] While it is true that a stronger inversion leads to a higher selectivity, the latter might be limited for conduction type inversion in silicon compared to state-of-the-art diffused junction or SHJ solar cells. However, in the light of the open-circuit voltages obtained in the past for MIS silicon solar cells, which reached values of 655 mV with inferior passivation layers, we expect the main limiting factor for our solar cells to be the ones discussed above.[85, 129]

### 3.5.6 Optical FDTD simulations

Figure 3.11 show the simulated (FDTD) reflection, transmission and absorption values for a metal nanowire network. The network absorbs on average about 10% of the incident light across the visible wavelength range.
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Figure 3.11: Simulated reflection, transmission and absorption. Simulated (FDTD) reflection, transmission and absorption values for metal nanowire network with a thickness of 50 nm (10 nm Pd, 40 nm Au), width of 100 nm, pitch of 1 μm.

3.5.7 Tunnel resistance

The resistance of the interfacial layer is non-linear in nature. For low intensities and insulator thicknesses below 1.5 - 2 nm, the $I_{sc}$ is limited by the semiconductor; all charge carriers are extracted and only an increase in intensity can increase the current further. Tunneling resistance is insignificant in that region, as the rate of tunneling is relatively low. For larger insulator thicknesses or higher intensities, the device characteristics shift from a semiconductor-limited to a tunnel-limited regime.[120] Because we observe a linear increase of the $I_{sc}$ and the efficiency throughout the investigated regime the contact resistance is not tunnel-limited.

Figure 3.12: Efficiency and short-circuit current vs incident light intensity. The measurements show that the contact is not tunnel-limited under 1 sun illumination conditions.
3.5.8 Annealing behavior

After the fabrication of our samples we encounter s-shaped I-V curves (Fig. 3.13(b)), which indicate charge carrier extraction barriers at the interface. Electron beam exposure of a-Si:H is known to cause the defects in the material.[119] As shown by others, and confirmed with our performed annealing experiments, those defects can mostly be removed by annealing the a-Si:H at around 220 °C for 30 min. In that temperature range the s-shaped I-V curves disappear and the measured $I_{sc}$ and $V_{oc}$ values after each subsequent annealing step (see Figure 3.13(a) and (d)) improve substantially. We reach a maximum for the $V_{oc}$ in the temperature range between 180 - 230 °C and an annealing time of around 30 min. However, the $I_{sc}$ and with it the $FF$ (not shown) do not reach a maximum but are monotonically increasing for the temperature and time range investigated. We choose to optimize the annealing conditions with respect to the $V_{oc}$ to be able to make conclusions with respect to the extent of the inversion layer. We note that, while the $I_{sc}$ and $FF$ of our solar cells could be better, based on the annealing experiments, we cannot exclude the possibility that the $V_{oc}$-value of our cells is reaching a value that is affected by the electron beam-induced damage in the a-Si:H.

![Figure 3.13: Annealing behavior. Influence of post-fabrication annealing steps on the $I_{sc}$, $V_{oc}$ and charge carrier extraction barrier at the interface. The subsequent annealing steps are listed in (c). (a) The measured $I_{sc}$ (blue) and $V_{oc}$ (green) values as a function of the annealing step. As can be seen, the $V_{oc}$ increases before reaching its maximum for an annealing temperature between 180 - 230 °C, and an annealing time of around 30 min. (b) With increasing annealing temperature and time the s-shaped IV curve disappears. (d) The $I_{sc}$ increases monotonically without reaching a maximum in the range investigated.](image-url)