Interfaces in nanoscale photovoltaics
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In this chapter we explore application opportunities that emerge out of our insights from the preceding chapters. Our increased knowledge about the internal workings in InP nanowires, especially with respect to selective contacts, allows us to propose a novel manufacturing process for nanowire solar cells. This process exploits the intrinsic advantages that emerge out of the nanowire geometry compared to thin-films; faster growth speeds, reduced material consumption, fast mechanical peel-off and intrinsic anti-reflection properties. We perform a techno-economic analysis of our proposed fabrication process by comparing the process to an already commercialized and very similar manufacturing process for thin-film GaAs solar cells. We include different nanowire growth methods that could be utilized for our proposed process and show that they have an enormous potential to reduce the manufacturing costs compared to MOVPE thin-films. The ability to discuss different growth methods points towards another important characteristic; the process line is highly flexible and not limited to one growth method, let alone semiconductor. We argue that this can have a substantial impact on the rate of innovation in a hypothetical company invested into this process. For future portfolio expansions we envision all-nanowire tandem configurations and III-V nanowires on silicon, all realized with essentially the same fabrication process. We close by proposing a roadmap for future developments and commercialization.
6 A nanowire solar cell fabrication process

6.1 Introduction

Here, we explore valorization opportunities that emerge out of our insights from the preceding chapters. In Chapters 4 and 5, we have conducted fundamental studies on horizontally aligned and isolated single InP nanowire devices. Those fundamental studies have increased our understanding about the thermodynamic limitations and especially about prevailing loss mechanisms. We not only quantified the impact of non-ideal contacts and non-radiative recombination on the device performance; we also showed first results towards reducing those loss channels. Previously, high quality contacts in terms of selectivity and Ohmic resistance have been an unresolved challenge for p-type InP nanowires, because of limited p-type dopant concentration and Fermi level pinning at the surface.

Those findings have implications far beyond fundamental studies on the single nanowire level. For practical devices, large arrays of vertically aligned nanowires have to be employed. The intricate optical characteristics of nanowires require precise alignment and ordering of the nanowire arrays to optimize absorption and emission properties. The current record holders are arrays of GaAs (15.3%) and InP (17.8%) nanowires.

Those nanowire array solar cells employ a single crystalline and highly doped substrate (GaAs or InP) for the nanowire growth and to establish electrical contact to the p-type part of the wires. As a result, even though nanowires are employed that principally could reduce the required material volume due to their optics, the final solar cell utilizes nanowires in addition to a costly substrate. Furthermore, the substrate provides a high density of optical states that lead to increased light emission into the highly doped and hence recombination active region. Those substrate related drawbacks have spurred interest in ways to separate nanowires after the growth from the substrate while maintaining the highly ordered array geometry. This is especially important in view of economically feasible applications.

It has been shown that nanowire arrays can be embedded in polymers and peeled off from their substrates to make suspended flexible foils. However, the unresolved issue of the challenging contact formation for p-type InP nanowires has created a stand still at this front.

In this thesis we have overcome this obstacle by finding ways to form highly selective contacts with a low contact resistance. Enabled by those fundamental findings, we lay out a pathway towards practical nanowire array solar cells: we propose an industrial manufacturing line.

We start by describing the fabrication process in technical detail and by discussing the expected and forecasted solar cell performance. The InP nanowires of the two preceding chapters have been obtained via selected-area metal-organic vapor phase epitaxy (SA-MOVPE). In our analysis we also discuss close space vapor transport (CSVT) and top-down etching as two alternative fabrication methods and extend our analysis to GaAs nanowires.

Starting from first principles it is challenging to estimate the technical feasibility of a large scale production and especially the future cost of a fabrication process.
Therefore, we compare our proposed fabrication process to a very similar and already commercialized one: flexible, high-efficiency thin-film GaAs solar cells (Fig. 6.1).[176] The general fabrication steps are known and allow for a sound estimate of the technical feasibility of our proposal.

To estimate the future costs of our technology, we rely on a cost model that has been developed by NREL for thin-film GaAs solar cells.[175] It allows us to conduct a techno-economic comparison to GaAs thin-films. However, the cost model by NREL has been developed under the same constraints, that is with limited knowledge about the undisclosed fabrication parameters. Therefore, we end our cost analysis with a relative cost comparison, underlining the most important cost factors (material usage, growth method and speed and peel-off speed). We are able to show that nanowire solar cells can reduce the costs relative to commercialized GaAs thin-film solar cells, even though the exact costs are unknown.

We discuss competing technologies and the emerging multi-billion dollar markets for electric vehicles and the internet of things. We forecast that those markets will be crucial for next generation solar cells, because they allow commercialization and development without forcing new companies to immediately compete against the mature silicon solar cell technology on a commodity market.

Finally, we discuss another very important feature: the process is highly flexible because it is largely independent of the exact growth process and semiconductor. This is in strong contrast to traditional solar cell fabrication processes, which are highly specific and limited to the employed semiconductor. The origin of that feature can be found in the very nature of the process. It exploits the intrinsic advantages that emerge from the nanowire geometry compared to thin-films; fast and flexible growth, reduced material consumption, fast mechanical peel-off and intrinsic anti-reflection properties. We close with a roadmap for the future.

Figure 6.1: Similarity of the fabrication processes for GaAs thin-film and nanowire solar cells. Upper pictures are taken from [175].
6.2 Process overview

In the following, we sketch out the fabrication process for InP nanowire solar cells grown by SA-MOVPE as this growth method has been used to grow the high quality nanowires in the preceding chapters. The process is however very flexible and can be expanded with minor adaptations to other materials (e.g. GaAs) or other growth methods, e.g. top-down etching, as we will discuss in detail below.

Figure 6.2 shows an overview of the proposed fabrication process, which starts with a single crystalline p-type InP wafer (Fig. 6.2(a)). The wafer is coated with a SiN mask, which can be patterned on a large scale by soft imprint lithography and top-down plasma etching (Fig. 6.2(b)). This patterned high quality substrate wafer is the basis for the following steps and can be reused multiple times.

The patterned substrate is moved into a MOVPE reactor, where precursors flow into the chamber at a specific rate, temperature and pressure (Fig. 6.2(c)). For the growth of InP nanowires, trimethylindium and phosphine are used. Additionally, p-type (n-type) doping of the nanowire end parts can be achieved by flowing diethylzinc (ditertbutylsilane) into the chamber. The final nanowire geometry consists of the n-doped nanowire tip on the top, an intrinsic part in the center and the p-doped part at the bottom, in contact with the p-doped substrate wafer. As we showed in the previous chapter, new selective contacts have the potential to remove the doping step and with it the encountered difficulties for the nanowire doping.

Then, the nanowire array is moved out of the MOVPE reactor and either into a chemical bath or directly into a plasma-enhanced chemical vapor deposition (PECVD) or ALD system to coat the nanowires with sulfur-based precursors and SiO₂. Both steps passivate the wurtzite InP surface (Fig. 6.2(d)). In the future, we expect this step to be a purely vapor phase method, as the functionalization of the InP surface with sulfur atoms is not restricted to solution-based methods.

After the surface passivation, the nanowire arrays are coated with a flexible polymer by spin, dip or spray-coating, after which a short O₂ plasma etch step is used to remove residual resist on the n-doped top part of the wire (Fig. 6.2(e)).

Now the back contact can be fabricated by standard metal evaporation. To improve film stability, the metal layer can be made thicker, either in a double layer or even single layer configuration 6.2(f).

In the next step, a thick and flexible polymer or glass handle is applied which binds tightly to the metal. The embedded nanowire array is then mechanically peeled-off from the substrate 6.2(g). This process step can be very fast, as it does not require chemicals to dissolve a buffer layer, as for epitaxially grown thin-films.

The substrate is now chemically cleaned from the polymer and can be reused many times, as the actual InP base material is not attacked 6.2(g-b).

The peeled-off flexible nanowire film has to be contacted right after the peel-off step by evaporating a thin and transparent film of MoOₓ, followed by a thicker TCO layer to facilitate the p-type contact (Fig. 6.2(h)).

This process can essentially be applied to many different semiconductor nanowires.
6.2 Process overview

Figure 6.2: Process overview of nanowire solar cell fabrication. (a) P-type InP substrate wafer, (b) patterned SiN coating, (c) MOVPE growth of InP nanowire array, (d) surface passivation, (e) polymer coating and short O\textsubscript{2} etch, (f) n-type metal contact, (g) mechanical peel-off step and (h) transparent p-type InP TCO contact and metal contact fingers. The patterned substrate (b) can be recycled many times as it only requires a short chemical etch between (g) and (b). This envisioned process is not limited to InP, but can be extended to other semiconductors, such as GaAs or GaInP, as well.
6.3 Technical details

6.3.1 Substrate patterning

As we discuss below, for SA-MOVPE and CSVT growth the InP wafer has to be coated with a SiN masking layer (e.g. by PECVD), and subsequently patterned by a large scale lithography process such as soft imprint or the related substrate conformal imprint lithography (SCIL).[177, 178] For soft imprint lithography a flexible stamp, which has been obtained by casting a polymer over a master, fabricated by electron beam lithography, is pressed into the resist layer. Then the resist is cured (heat or UV) and the stamp released. A short O\textsubscript{2}-descum step is added to remove residual resist on the bottom of the nanoscale indentation. This technique allows for a low-cost but large scale patterning of nanoscale features with dimensions > 100 nm. Since the nanowires have diameters in the range of ~ 100 – 200 nm and the arrays pitches of ≤ 500 nm, soft imprint lithography has a sufficient resolution.

6.3.2 Growth methods

In the following we shortly summarize competing technologies for the fabrication of nanowire array solar cells. As mentioned above, one of the great advantages of this fabrication process is its high flexibility.

**Top-down etching**

The first method relies on top-down plasma etching of nanowires into a substrate wafer via an etch mask. The plasma etching in research reactors can be relatively fast for inductively coupled plasma etching (~ 2 μm/min).[179] As described in the cost section, the material costs for nanowires that are obtained by top-down etching into bulk wafers can be lower compared to many other growth techniques. Even though the etching consumes up to 80% of the wafer (depending on the exact geometry), the cost per unit volume is substantially cheaper than for MOVPE thin-films. While the patterning step of the etch mask needs to be repeated with every step, nanosphere lithography is a low-cost and large-scale method which can be employed for that purpose.[180, 181] An open question is the quality of the substrate wafer, especially for GaAs, which can vary largely depending on the growth method employed.[182] While liquid encapsulation Czochralski (LE-CZ) and the vertical gradient freeze (VGF) methods can provide single-crystalline wafers, the high-purity requirements for high-efficiency solar cells are more demanding. Most of the current applications of GaAs wafers have different requirements, such as a very high carbon concentration which leads to Fermi level pinning at a mid band gap defect state and hence a semi-insulating wafer (SI GaAs). The vast majority of available GaAs wafers has specifications unsuited for efficient solar cells.

InP wafers can be obtained at a desired quality, however they are more expensive due to reasons mentioned in the cost discussion.
CSVT

Close-space vapor transport (CSVT) is a growth technique which uses \( \text{H}_2\text{O} \) vapor to etch a solid GaAs source and thereby generates the vapor-phase reactants As\(_2\) and Ga\(_2\text{O} \) at atmospheric pressures. Those in situ generated precursors diffuse driven by a thermal gradient towards the cooler substrate and deposit as GaAs. The substrate is spaced closely (< 1 mm) from the source, which results in a high precursor utilization of up to 95% and a high growth rate of up to 1 \( \mu \text{m/min} \). Additionally, the reactors can be built relatively cheaply and the growth principle allows for very fast and large batch processing.[183] In fact, the reactor design is very similar to already commercialized reactors that are employed for CdTe growth. Recent developments showed the high potential of CSVT as a viable technique for future industrial applications, with epitaxial GaAs thin-films on par with commercial single crystalline wafers and selective area epitaxy of GaAs microstructures.[183–185] So far, selected-area epitaxy of nanostructures has not been shown, but current developments are very promising.

Figure 6.3: The MOVPE reactor. The reactor utilizes gas precursors such as trimethylindium and phosphine to grow semiconductors inside the deposition chamber. The gases are entering the chamber via a diffuser and mixing chamber that, together with the rotating substrate wafers, guarantee a homogeneous deposition. The MOVPE reactor is highly flexible as many different precursor gases can be utilized for the growth of a wide range of semiconductors. Taken from NREL.[175]
SA-MOVPE

Selected area metal-organic vapor phase epitaxy (SA-MOVPE) growth relies on the fact that materials like InP and GaAs can be grown epitaxially along the (111) direction of a substrate wafer. To obtain nanowires the substrate is covered with a mask that only allows the nanowire growth in selected areas.\[186\] For research reactors, the growth rate is relatively slow (~ 0.2 \( \mu \text{m/minute} \)), however about 5-10 times faster than the thin-film growth (~ 0.02 \( \mu \text{m/minute} \)). Industrial reactors have shown increased growth rates for epitaxial thin-films of up to (~ 0.25 \( \mu \text{m/minute} \)) and likely above (but undisclosed).\[176\] Assuming similar precursor utilization efficiency between thin-film and nanowire growth (which is commonly seen), simple conservation of matter arguments lead to a growth rate 5-10 times higher for nanowires (depending on exact nanowire diameter/pitch).

Figure 6.3 shows a schematic of a MOVPE reactor, taken from a publication by NREL [175]. As can be seen, the MOVPE reactor consists of multiple gas sources, transport lines, mass flow controllers and valves which deliver the desired gases to the growth chamber. Entering the growth chamber, the precursors are delivered into the chamber at a specific flow rate, temperature and pressure. For the growth of InP nanowires, trimethylindium and phosphine are used. Additionally, p-type (n-type) doping of the nanowire end parts can be achieved by flowing diethylzinc (ditertbutylsilane) into the chamber.

A commercial MOVPE system can hold up to 8\( \times6" \) or 15\( \times4" \) wafers [175] and is estimated to provide a precursor utilization of currently ~ 30\% for the group III sources (Al/Ga/In) and ~ 20\% for the group V sources (N/P/As/Sb).\[175\] Main loss sources are side wall deposition in the plumbing system and deposition chamber, as well as the venting and purging processes via the waste line.

One of the great benefits of a MOVPE reactor is its versatility; because the material is delivered via gas precursors the growth is expandable to other materials, simply by switching the precursors and substrate wafers. Among those alternatives are GaAs, GaP, InGaP and GaN.

6.3.3 Surface passivation

As also shown in Chapter 5, the surface recombination of nanowires can be lowered by specific surface treatments, even for InP with its low intrinsic surface recombination. These treatments can passivate the surface chemically or via the field-effect, that is interface charges that repel minority carriers. Therefore we include an extra passivation step in the proposed fabrication process (Fig. 6.2(d)).

6.3.4 Polymer/glass coating

The passivated nanowire arrays have to be coated with a flexible polymer (e.g. PDMS) or with a solgel matrix (\( \text{SiO}_2 \)), depending on the mechanical response in the following lift-off step (Fig. 6.2(e)).
6.3 Technical details

6.3.5 The contacts

So far, nanowire array solar cells use indium tin oxide (ITO) to contact the n-type InP nanowire tips, while the p-type contact can only be established via the p-type doped substrate. This limitation has hindered the development of nanowire array solar cells towards industrial application. The unresolved problem of contacting the p-type InP part, other than via the substrate, has prevented the realization of a substrate-less InP nanowire array solar cell based on a lift-off process.

During the course of this thesis, we were able to successfully contact p-type wurtzite InP and realized record performance single nanowire solar cells. Furthermore, we showed not only that the p-type part can be contacted via a metal layer (Chapter 4), but also via MoO$_x$, a high work function interfacial layer (Chapter 5). Besides realizing a high quality contact, those two findings add flexibility:

nanowires can be grown either with a p-i-n or n-i-p doping profile. In both cases the transparent or the continuous metal contact can be applied before or after the lift-off step. This is a very flexible scheme and the final fabrication process is likely to be determined by mechanical properties of the exact employed materials.

Increasing efforts are made in the development of flexible TCOs, encompassing ITO with the addition of sparse metal nanowire networks.[170, 171] Therefore, we forecast that the continuous metalization on one side will eventually be replaced by a flexible TCO in the near future. This will allow the fabrication of flexible and transparent (for $E < E_g$) nanowire array solar cells, which will be an important step towards the realization of nanowire tandem foils.

Figure 6.4: Electron and hole contacts. A continuous metal film is deposited first, followed by a transparent contact after the mechanical peel-off step. However, due to the flexibility of the contacting and the nanowire growth the geometry can be reversed.
6.3.6 Mechanical peel-off

The mechanical peel-off step as shown in Figure 6.5 allows the targeted breakage of the nanowires at the bottom, just above the substrate, and has already been used to make solar cells and LEDs[170–174] Because this step relies on mechanical breakage and the lower adhesion of the polymer to the SiN mask than to the metalization on the top, it is substantially faster than chemical lift-off steps which include a waiting time of up to several hours for the chemicals to dissolve a release layer. This leads to a strong bottleneck for fabrication processes employing chemical lift-off procedures and can be circumvented by a mechanical peel-off step for our nanowire arrays.

We stress that while the other proposed fabrication steps can employ industrially proven processes, the mechanical peel-off step needs further development. Even though the feasibility has been proven in research labs, it needs to be translated to a roll-to-roll process, optimized for nanowire array thin-film mechanics.

6.3.7 Solar cell performance

The current power conversion efficiency record for InP nanowire array solar cells is 17.8%, obtained by top-down etching into a previously grown MOVPE layer.[13] In this thesis we have already shown that higher open-circuit voltages than for the record solar cells are achievable which brings efficiencies of 20% certainly within reach, especially considering further optimizations in terms of doping profile and contact selectivity. Further improvements in reduced surface recombination
are likely to eventually move InP nanowire solar cells beyond the 26% efficiency record obtained for silicon solar cells. Considering the band gap of the material (for wurtzite InP 1.43 eV) and Auger recombination, InP nanowire solar cells are limited to an efficiency limit very close to that of GaAs \( (E_G = 1.42 \text{ eV}) \).[17, 161] However, due to the a more gradual absorption onset at the band gap (wider Urbach-tail), the actual efficiency limit is reduced slightly compared to GaAs.[187]

Even though GaAs nanowire solar cells have a higher theoretical efficiency limit, the record of 15.3%, obtained by the VLS growth method, is below the one for InP nanowires. This has to be ascribed to differences in the growth method and the higher intrinsic surface recombination velocity in GaAs compared to InP.[14] This underlines the importance of proper surface passivation layers for future efficiency increases, as discussed in Chapter 5.

Another efficiency boost related to the device architecture can be expected with the removal of the high refractive index substrate. In the radiative efficiency limit the emission towards the substrate which provides a high density of optical states \( (n^2 \times R_{rad}) \) is a loss channel (Fig. 6.6(a)). If the emission can be reduced by removing the substrate, the radiative \( V_{oc} \) will be higher (Fig. 6.6(b)). Furthermore, if a metal back contact is used as in the current version of the proposal, an increase in the directivity of the black body emission from the cell can be expected (Fig. 6.6(c)). The metal acts as a mirror and prevents emission to the bottom.[20]

**Figure 6.6: Substrate influence on the efficiency.** (a) Increased light emission from the nanowire into the highly doped and recombination active InP or GaAs substrate provides a large loss channel. (b) Removal of the high-index substrate reduces the emission towards the bottom. (c) An additional mirror improves the directivity by reflecting emitted light back through the array. Eventually the light can only escape into the upper hemisphere.
6.4 A techno-economic comparison to commercial GaAs solar cells

Starting from first principles, it is challenging to estimate the technical feasibility of a high-throughput and large scale production and especially the future cost of a fabrication process. Therefore, we chose commercial GaAs thin-film solar cells (28.8%) as a cost benchmark. The choice stems from the similarity of the growth process: the films are MOVPE grown GaAs with a thickness of 1-2 \( \mu \text{m} \). A release layer that has been grown before the actual device layer is etched away in a subsequent chemical lift-off step. The result are defect-free high quality GaAs thin-films.

6.4.1 Technology

As already discussed in the introduction, the fabrication processes for the proposed nanowire solar cell and the GaAs thin-film solar cell are very similar.

The MOVPE nanowires and thin-films are grown on a monocrystalline substrate wafer (GaAs or InP). The major MOVPE part in terms of material usage, time and cost (see below) is the growth of the GaAs base layer (out of trimethylgallium and arsine) and of the low to intrinsically doped part of the InP nanowires (out of trimethylindum and phosphine). The nanowire geometry provides intrinsic nanophotonic effects, such as optical cross sections that extend beyond the geometrical ones. As a result, the required material for a layer that absorbs close to all of the light is roughly reduced by a factor of 5 for the case of nanowires (assuming a nanowire diameter of 200 nm, pitch of 500 nm and a length of 2 \( \mu \text{m} \)).

Furthermore, the SA-MOVPE growth of nanowires allows for growth rates that are 5-10 times faster, compared to growth rates for thin-films. For the rest of the comparison we assume the lower bound, that is a factor of 5.

Lastly, the lift-off steps differ strongly. The epitaxial GaAs thin-film and the substrate wafer are separated by a thin AlAs buffer layer, which is slowly etched away during the lift-off (~ 2h). In strong contrast, the mechanical peel-off step for the nanowire arrays can be substantially faster. Fig. 6.7 shows a summary of the technical comparison.
6.4 A techno-economic comparison to commercial GaAs solar cells

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Figure 6.7: Summary of technical comparison An overview about the technical comparison between commercial thin-film GaAs and the proposed nanowire solar cell fabrication process, including different growth methods.

6.4.2 Economics

While the above comparison shows the technical feasibility, the area of economics is naturally tainted with more uncertainty. We use a cost model that has been developed by NREL for GaAs thin-film solar cells and adopt it for our proposed nanowire solar cell fabrication process.[175] As a result, we can pinpoint the most important differences and their impact of the production costs.

Figure 6.8 shows a summary of the cost analysis in a bar diagram for 29% efficient GaAs thin-film solar cells (blue), taken from [175], for 15% efficient InP nanowire cells (green), 15% and 29% efficient GaAs nanowire cells (orange and red). Also included are the estimated costs for top-down etching (vertical lines) and CSVT (horizontal lines). Material costs are shown in a bright color and depreciation, labor and maintenance costs in a dark color tone. The costs for the chemical GaAs thin-film lift-off step as stated by NREL are relatively uncertain.
(red question mark), because a particularly slow process step necessitates a large process parallelization which can lead to other complications, such as a large factory footprint.

We note, that the assumed efficiencies for our cost analysis have not been achieved for the considered growth methods, yet. However, efficiencies of around 14% and 15% have been achieved for VLS grown InP and GaAs nanowires, and 17.8% for top-down etched wires (into a MOVPE grown layer).[13, 14, 23] As we have shown in this thesis, SA-MOVPE nanowires have the potential to reach efficiencies of $20 - 30\%$, certainly with improved surface passivation and contact selectivity.

For the reusable substrate wafers, we forecast a cycle number that is equal to, if not higher than, the estimated ones for GaAs thin-film growth ($\sim 500$). The substrate wafer is almost completely protected by the SiN layer for SA-MOPVE or CSVT. As a result, the occurring substrate costs are not decisive in our cost comparison, except for the growth of InP nanowire by SA-MOVPE. The latter is strongly affected by the higher costs of InP wafers, as discussed in the section for top-down etching. However, one approach to reduce the costs substantially and even realize tandem solar cells in the future is the growth of III-V nanowires on silicon.[188] While the lattice mismatch of many materials makes epitaxial and dislocation-free growth of
thin-films impossible, nanowires exhibit the advantage of strain relaxation through the nanowire sidewalls. Therefore, a vast expansion of the material space allows not only to vary the material of the nanowire itself, but also of the substrate.

While our cost calculation includes all the different growth steps, we focus in the following on the decisive cost factor: the absorber growth. The detailed information about the raw materials, substrate wafers, the lift-off and the contacts can be found in the supplemental information.

**Growth: MOVPE**

GaAs thin-films and SA-MOVPE nanowires rely on the same growth method, which is dominated by two major cost factors. The first one is related to the expensive reactors, which provide a highly homogeneous and controlled growth environment. The depreciation and labor costs associated with the MOVPE reactor are among the highest of the whole fabrication process. These costs have been obtained for a growth rate of \( \approx 0.25 \mu \text{m/min} \) for GaAs thin-films. As mentioned above, we assume that the nanowire growth is approximately five time faster, based on comparisons for research reactors. Therefore, for a constant process output, up to five times less equipment is needed (neglecting reactor pumping, purging and venting times). This in turn leads to a substantial reduction in forecasted depreciation and labor costs of the MOVPE reactors for the nanowire growth compared to the GaAs thin-film growth.

Besides comparing the depreciation and labor costs, the material costs for the precursors have to be considered. Assuming the same precursor utilizations of 30% and 20% for the III-source (Ga/In) and the V-source (As/P), the required amounts of material will be reduced by a factor of 5 for the nanowire arrays. However, trimethylindium is about 10 times more expensive than trimethylgallium. The reason can mainly be found in the lower demand and could therefore substantially be reduced if demand would pick up, as is the case for the substrate wafers and the raw metals above. In contrast, arsine and phosphine are very similar (and low \( \approx 0.04 \$/W \)) in price.

Accounting for the different efficiencies (29% for the GaAs thin-film and 15% of the InP nanowire array), the lower depreciation and labor and higher material costs, we estimate the cost for the MOVPE step for the InP nanowire arrays to be \( \approx 2.21 \$/W \) compared to \( \approx 2.45 \$/W \) for GaAs thin-films. Assuming a drop in price for trimethylindium towards that of trimethylgallium the price will be as low \( \approx 0.7 \$/W \). Those costs are expected for 15% efficient GaAs nanowire solar cells.

**Growth: top-down etching**

For top-down etching, the estimated nanowire fabrication costs are calculated in a straight forward way. We assume a nanowire lengths of 2 \( \mu \text{m} \) and another 1 \( \mu \text{m} \) due to plasma damage of underlying substrate and the polishing steps. The 1 \( \mu \text{m} \) buffer layer has to be etched away before the next patterning and growth step. Therefore,
~ 3 μm of the initially 600 μm thick substrate wafer are consumed per nanowire array, that is 200 arrays can be obtained from one wafer. The 6” GaAs wafer can be cut into pseudo-square shape with a 133 cm² area (27% loss). Taking into account the different conversion efficiencies and the illumination intensity of 100 mW/cm², the costs in $/W can be calculated. The InP wafers are currently a factor of four more expensive than GaAs wafers. There are three main reasons for this difference, taking into account that the raw material prices of Ga and In are similar in price: (1) growing InP wafers requires higher pressures and temperatures than GaAs, (2) InP wafers are more brittle and hence lead to more accidental breakage during the handling and most importantly, (3) there is no commodity market for InP so far. This is in strong contrast to GaAs, which is used in several applications, e.g. in power amplifiers of cell phones, and can therefore benefit from economies of scale and more developed and specialized process equipment. Obviously, increasing InP demand would drive the cost down in the long run, eventually substantially narrowing the price gap to GaAs. However, for top-down etching of GaAs nanowires, the cost estimates are rather optimistic, because we assumed the same prices for the substrate wafers as in the case of the epitaxial growth. While the wafers have a high crystalline quality, the impurity content for most available GaAs wafers is completely unsuited for the use as photovoltaic absorber (see also 6.3.2). Therefore, a substantial increase in price can be expected.

Another issue is the use of one homogeneously doped bulk wafer for the fabrication of hundreds of nanowire arrays. Unless selective contact layers or doping via post-growth annealing are employed, no practical solar cell can be fabricated.

Keeping those uncertainties in mind, the cost of the etch process for a hypothetical 29% GaAs nanowire solar cell are around 0.25 $/W and around 2 $/W for 15% InP nanowire solar cells, due to the lower efficiency and higher substrate costs.

The costs of the etch step itself are rather low. Plasma etching is an industrially proven technology, e.g. for the edge isolation of silicon solar cells. Therefore, the cost for the equipment are estimated to be small, at 0.02 $/W for the 29% GaAs nanowire array.

**Growth: CSVT**

CSVT has been developed in 1963, but its potential has only recently been demonstrated. Therefore, the potential costs of industrial fabrication can only be roughly estimated. The major difference for CSVT growth compared to the other methods are the material and the reactor costs. Instead of using expensive (and toxic) precursors, such as trimethylgallium (~ 2.5 $/g) and arsine (~ 0.4 $/g), CSVT can directly utilize high purity gallium (~ 0.5 $/g) and arsenic (~0.1 $/g). Additionally, a CSVT reactor is very similar to reactors employed for the fabrication of CdTe solar cells. Especially the close space sublimation (CSS) and the vapor transport deposition methods have strong similarities to CSVT. Considering that the growth is only a fraction of the module manufacturing process, the costs for the CdTe deposition method are at about 0.06 $/W for an efficiency of 16%.
If the assumption holds, that CSVT nanowire solar cells can be grown directly out of Ga and As with a very similar process as employed for current CdTe manufacturing, the overall costs for the growth step are around 0.2 $/W for a hypothetical 15% efficient nanowire solar cell and only 0.1 $/W for a 29% cell.

**Overall absolute and relative costs**

Adding up all the costs, including final edge isolation, testing and sorting (~ 0.05 $/W) the 29% efficient GaAs thin-film can be produced at about ~ 3.3 $/W. Compared to reference [175] we assume the same costs for the front and the back side metalization. For the scenario a 500 MWp U.S. facility with a 95% yield and 5 year equipment depreciation time have been considered (mid-term single-junction case in [175]). For a nanowire solar cell facility with the same assumption, a 29% efficient SA-MOVPE GaAs nanowire solar cell could be produced at a price of about ~ 0.88 $/W. For a SA-MOVPE InP nanowire solar cell with an efficiency of 15%, the total cost would add up to about ~ 4.95 $/W, strongly affected by the high wafer and precursor prices compared to GaAs.

For top-down etching, the 15% InP nanowire solar cell could be produced at ~ 3.43 $/W and the 29% GaAs nanowire solar cell at ~ 0.78 $/W.

For CSVT, the 15% GaAs nanowire solar cell could be produced at ~ 1 $/W and the 29% GaAs nanowire solar cell at only ~ 0.5 $/W.

The absolute cost estimates have a high uncertainty, due to undisclosed information. As Alta Devices has developed their fabrication process over several years, it is almost certain that lower costs are reached. Therefore, we show in Figure 6.9 the relative costs of the MOVPE nanowire solar cell to the thin-film GaAs fabrication. The cost difference between the different GaAs technologies is largely due to the large differences for the MOVPE process step, with nanowires using roughly 5 times less material and a having a growth rate that is about 5 times higher than for thin-films. For InP the high costs for wafers and precursors relative to GaAs are a high obstacle for an economic production, but could be reduced substantially if demand would pick up. We conclude that the nanowire solar cell fabrication is not only technically but also economically a highly promising proposal.

### 6.5 Markets and competitors for nanowire photovoltaics

#### 6.5.1 The perseverance of the silicon module

Flexible InP or GaAs nanowire solar cells are likely to exceed the efficiency records of silicon solar cells due to their higher Shockley-Queisser efficiency limits and intrinsic nanophotonic effects in the future. Furthermore, they have the added benefit of being light weight and potentially flexible, important points when it comes to shipping and installation.
However, the maturity of the established production processes and the economies of scale of the wafer-based silicon solar cell technology create large obstacles for new technologies to enter the market. Currently, solar module prices are as low as 0.57$/W with further substantial cost reductions expected in the upcoming years. Improvements on the module efficiency level, optimized processes and further economies of scale are the main driver of this continuing decrease of solar panel productions costs over the years. As a result, the cost of solar energy for fully installed systems is predicted to fall below 1 $/W by 2020 and down to 0.3-0.7 $/W by 2050.[16] As a comparison, in Chapter 6.4.2 we have argued that the MOVPE step alone, will initially be more expensive than the whole silicon solar cell fabrication and installation together, even for a GaAs nanowire geometry. This clearly shows that in the initial development stages and without economies of scale, such new technologies are unable to compete on the same market as the established silicon solar module. Unless a new solar cell technology is developed that can be fabricated with substantially cheaper processes, such as solely with chemical batch processes, the predominance of the silicon solar cell module is to be expected in the near and midterm future.

Nevertheless, new technologies can successfully be commercialized if they do not compete, at least initially, on the same market as the silicon solar module.

### 6.5.2 Flexibility, light-weight and efficiency

Unmanned, lightweight systems, such as aerial drones, consumer devices, such as smart phones, computers, clothes, watches, and cars are providing a large market for new technologies where $/W is not the most important figure of merit.
Other numerous applications emerge via the upcoming internet of things (IOT), a term that describes the increasing connectivity of a wide range of devices to the internet. The IOT are forecasted to become a multi-billion dollar market in the near future, mainly driven by the continuous decreasing costs of computer chips and data storage and transmission costs. The same holds for the market of e-mobility, with recently almost all major car companies announcing major developments and even upcoming product introductions. This is in stark contrast to even ten years ago, where light weight and flexible solar cells were only envisioned for small and sometimes exotic “niche” markets, such as for remote power supply of weather stations. If the current economic forecasts hold, we are just at the beginning of the emergence of two multi-billion dollar markets.

If weight, flexibility and high-efficiencies are the major requirements for applications, great opportunities are arising for new solar cell technologies, that can provide those functionalities. In the long term, such technologies can then try to compete against the existing silicon solar cell when maturity of processes and economies of scale can impact the $/W figure substantially.

### 6.5.3 Competitors

Flexible and especially light-weight solar cells are not a new concept per se. The advantages of such a technology in terms of transport, installation, module costs and application space have spurred continuous interest in this promising device architecture. So far, flexible and light-weight solar cells have been realized for organic and amorphous silicon solar cells (~10%), CdTe (~16%), CIGS (~23%) and GaAs thin-films (~29%) [17, 198, 199].

Commercial organic solar cells can be produced very cheaply via solution-based methods but are currently limited in efficiency and stability. For amorphous
silicon, evidence in mounting for years, that stable inherent crystal defects strongly limit the performance, making high-efficiencies likely beyond reach.[200].

Flexible CdTe and CIGS solar cells can provide a stable performance in the low to mid-efficiency range and are therefore main competitors to our proposed solar cell technology in the initial stages. For flexible CdTe films, a safe and leakage-free containment of the material has to be found, especially if the technology is to be employed in close proximity to the end-user.

Alta Devices thin-film GaAs solar cells are the most efficient (28.8%) single-junction solar cells available on the market and they have the benefit of being lightweight and flexible. Even though they provide all those benefits, they are currently too expensive to compete against the silicon solar cell module for large scale primary electricity production, as discussed above.

As for the proposed nanowire solar cells, one has to distinguish between the current status as in our proposal and future opportunities. Material developments are likely to increase the conversion efficiencies towards the values achieved for GaAs thin-films and process optimizations and economies of scale we lead to substantial cost reduction. Furthermore, full flexibility and even high transparency (for $E < E_g$) through the developments of new flexible TCOs are going to be important milestones for this technology.

Therefore, the targeted markets for CIGS, CdTe and GaAs thin-films solar cells are similar to the proposed nanowire solar cell technology. We envision nanowire solar cells that can be produced cheaper but are at least initially lower in performance (20% vs. 28%) than GaAs thin-film solar cells. As a result, we see a large market that can be accessed by nanowire solar cells, simplified, whenever lightweight and mid-range efficiency are more important than a high-end performance. Therefore, nanowire solar cells will at least initially compete against CIGS and CdTe modules about the same market share.

In the following we will argue that our flexible fabrication process allows to develop nanowire tandem solar cells to eventually reach substantially higher conversion efficiencies and thereby larger market shares.

### 6.6 Innovation by flexibility

#### 6.6.1 A traditional fabrication process

Traditional mono- and multicrystalline silicon, amorphous silicon, CIGS and CdTe solar cells have all a very common characteristic, in fact it is so common that it is barely discussed; they all rely on fabrication processes that are highly specialized for the employed semiconductors. The specific semiconductor growth process and the resulting geometry impose strong limitations on the whole fabrication process. The reason for that can be found in the large variety of material properties and hence requirements in terms of crystal growth, required semiconductor thickness, bulk- and surface defect passivation, electrical contacting and many more. This
setup adds to the unavoidable dilemma for traditional solar cell manufacturers.

Initially, for a newly commercialized solar cell technology, many companies can advance their products in terms of technical performance improvements (e.g. improving the efficiency or stability of their solar cells). Usually, technical know-how about certain details is even the main driving-force for technology start-up companies. However, after some time, fundamental physical limitations especially in terms of efficiency (e.g. Shockley-Queisser-Limit) and practical material limitations (e.g. limited carrier mobilities) change the rate and hence increase the costs at which improvements can be obtained. This fact becomes evident in Fig. 1.1 in Chapter 1, which shows the efficiency improvements of different solar cell technologies over time. The characteristic logarithmic trend of many mature solar cell technologies is pronounced. Notably, for mono- and multicrystalline silicon solar cells, which make up over 90% of all fabricated and installed solar cells, hardly any substantial efficiency improvements have been obtained over the last 20 years on the cell level (average module efficiencies increased substantially). At such developmental stages, a company that would aim to mainly improve the efficiency of their solar cells would have to invest enormous amounts of money in their R&D department. Taking into account the nature of research, that is the large uncertainty that comes with it, a silicon solar cell company is better advised to conduct its main efforts in other areas. This is why even technology companies focus with increasing maturity mainly on cost reductions driven by economies of scale and process improvements (speed, reliability, material consumption aso.). Consequently, the reason why the fabrication costs for silicon solar modules continued to drop in the past, even though the single cell efficiency barely improved, can mainly be attributed to economies of scale, more optimized process equipment and optimizations on the module level (leading to lower efficiency losses between cell and module). In other words: solar cell companies have installed a large amount of highly specialized equipment in ever increasing factory sizes. Neglecting internationally different environmental protection standards, labor rights and standards of living, silicon solar cell fabrication today is more efficient in terms of resources (energy, materials, labor) than 20 years ago. Without those developments the whole solar energy sector would still be in its infancy.

While it seems of utmost importance, if not a necessity, for a new technology to reach this stage of development, there comes a fundamental downside with it. Companies become less flexible and less likely to achieve breakthrough innovations the larger and older they get. It has been observed that companies increase the rate of patenting with age, however those patents are highly focused on a specific area of expertise and show a strong declining rate of external citations. In other words, companies show an increasing divergence between organizational competence and current environmental demands with age.[201] To maintain oversight and productivity, large companies have to rely on more bureaucracy and management layers per capita, standardizing internal procedures and specializing on a specific area of expertise. Thereby, they inevitably create barriers for breakthrough approaches.
However, not only the work force and its organization, but also the large amounts of equipment become highly specialized and optimized for the current manufacturing process. This in turn reduces the rate of innovation, as the existing fixed fabrication process does not allow for ground-breaking innovation. The technical improvements are only incremental. Single process steps can sometimes be replaced by more material, labor, time or energy efficient versions, but the end product stays effectively the same, e.g. a single junction silicon solar cell. Often the only way for large companies to stay truly innovative is to completely replace their product line, that is to sell or outsource the current technology and acquire new expertise and equipment through acquisitions and mergers.

To summarize, companies have to deal with large costs of a highly specialized workforce which is inflexible due to bureaucratic barriers and organizational structures. Additionally, the current technological setup strongly limits their phase space of explorations. Much attention is currently spend on ways to improve innovation and flexibility in a large work force by means of new organizational structures and incentives. In contrast, the impact of the nature of a specific fabrication processes on future innovations is not often discussed, especially not in the field of solar energy.

In the following, we will argue that our proposed fabrication process for nanowire solar cells is of very different nature, allowing a hypothetical company to stay more agile and innovative even if process maturity and large scale installations of manufacturing lines are realized.

### 6.6.2 A flexible fabrication process

Our proposed fabrication process is inherently different from the traditional manufacturing lines, as shown in Figure 6.11. It is highly adaptable and flexible and not limited to one specific semiconductor. It allows not only for the fabrication of nanowire arrays made out of InP, but also the fabrication of nanowire and even microwire arrays out of many other materials, such as GaAs, GaP, GaInP, GaN and many more. In fact, even LED panels can be envisioned as product portfolio extensions. To reach such a high level of flexibility for a solar cell fabrication process, three basic properties have to be provided by the process equipment:

**Flexible growth, flexible handling and flexible contacting of the semiconductor.**

For our process those features emerge because it exploits the intrinsic advantages of nanowires compared to thin-films; fast and flexible growth, reduced material consumption, fast mechanical peel-off and intrinsic anti-reflection properties.

The flexible growth is initially provided by the MOVPE growth system and the fact that nanowires have less stringent requirements for epitaxial growth than traditional thin-films. Together with a large range of available substrates many different semiconductors can be grown, as discussed in Chapter 6.3.2. However, the whole process is even more flexible in that it allows to replace the MOVPE growth steps with other methods, as discussed above. If CSVT growth of nanowires reaches maturity, the more expensive MOPVE equipment can be replaced, while the rest
of the process line only needs smaller adjustments. The mechanical peel-off, subsequent handling and the final module assembly are all largely indifferent to the exact semiconductor used. Since the nanowires are embedded in a polymer or glass matrix, the mechanics are largely determined by the latter.

Last but not least, the deposition equipment used to deposit the TCOs and the metal contact fingers can be used for a large range of materials. The ongoing development of flexible and high and low work function TCOs for carrier selective contacts, adds further simplicity and flexibility to the fabrication process.

Obviously, with every material change, the different fabrication processes have to be fine tuned, especially the growth step. However, the fact that different semiconductor solar cells can be grown at all with the same process line and that the specific growth method can even be switched out if cheaper alternatives are available (e.g. CSVT), allows a company to stay highly flexible. This is of prime importance, especially for a solar cell company.

Compared to many other fields, with unknown or less well-defined limitations, the well-known and well-defined physical limitations for solar cells create inevitable performance boundaries. The Shockley-Queisser and other material related limits, do not allow the continuous development in terms of higher conversion efficiencies with a set, given semiconductor. A company that can break through this limitation by e.g. developing a tandem solar cell, in parallel to the
fabrication of single-junction solar cells, has a tremendous advantage.

We want to stress that we do not underestimate the importance of organizational structures, bureaucracy and other work force related factors on the rate of innovation. As the innovative process starts on the human level, organizational structures that allow and incentivize the exploration of new approaches are the first step towards enabling breakthrough innovation. However, without technical abilities to turn those ideas into physical realities, innovation inevitable has to cease.

6.7 Conclusion and a technological roadmap

We have shown that the nanowire fabrication process is not only technologically but also economically feasible. The crucial fabrication steps are the utilization of a reuseable substrate, coupled to an epitaxial MOVPE growth and mechanical peel-off step. The proposed fabrication process is very similar to the ones employed for thin-film GaAs solar cells, with the major differences being a faster and more material efficient MOVPE growth and a faster mechanical peel-off step. However, we do not limit ourselves to the MOVPE growth method, but include other nanowire fabrication methods, too. Besides the technical aspects of the fabrication process, we also compare the economical ones with commercial thin-film GaAs solar cells. We are able to show that nanowire solar cells can potentially be fabricated cheaper. Based on our techno-economic analysis we are able discuss future market opportunities and competitors.

Besides this positive outlook for commercial nanowire solar cells, we arrive at another important insight; the proposed fabrication process for nanowire solar cells is highly flexible. Figure 6.12 shows a simplified roadmap for the technological developments and future markets of the respective technologies. As a result of the
flexibility of the manufacturing line, large synergies are created with each subsequent portfolio extension. GaAs nanowire solar cells would benefit from the prior realized substrate recycling, the peel-off process and the contacting and handling steps for InP nanowires. As a result, GaAs nanowire solar cells could enter commercialization after improvements in surface passivation and selective contacts, skipping phase 1-3. Eventually, further process optimizations and economies of scale could make an all nanowire or nanowire-on-silicon tandem solar cell feasible, which could directly compete against the existing silicon module.

6.8 Supplemental information to cost comparison

Raw materials

Between the years 2011 - 2015, the annual average prices for gallium ranged between 300 - 700 $/kg and for indium between 540 - 700 $/kg. The fact that gallium and indium can only be found in trace amounts as gallium and indium compounds in bauxite and zinc ores explains the tendencies towards higher prices. Further adding volatility to the prices, gallium and indium extraction are heavily dependent on aluminum, zinc and lead extraction and demand, because of the small amounts present in the deposits. For comparison, silicon is extracted from highly abundant SiO$_2$ which resulted in average annual prices for metallurgical-grade silicon of 2.6 - 3.5 $/kg in the years 2011-2015. Even though the prices are similar, the demand for indium, which does not have its own commodity market, is substantially lower than for gallium. As an example, while the US economy completely relies on imports for its Ga and In demand, it imported around 32,000 kg Ga compared to only 145 kg In in the year of 2015. Therefore, if In demand picks up in the future and a commodity market could be established, the prices of In will almost certainly go down.

Reusable substrate wafer

For MOVPE growth of thin-films and nanowires, as well as the CSVT growth and the top-down etching approach, the growth of the III-V substrate wafer has to be considered in the cost comparison. To purify the respective materials and grow single crystalline wafers the VGF or LE-CZ growth method can be employed (6.3.2). As mentioned and explained above, InP wafers are currently a factor of four more expensive than GaAs wafers. Adding to the costs for the substrate wafer are the costs for the SiN coating and the patterning step for SA-MOVPE and CSVT. However, we forecast a cycle number that is equal to, if not higher than, the estimated ones for GaAs thin-film growth (~ 500). The substrate wafer is almost completely protected by the SiN layer. After the peel-off a small amount of material that has been grown by MOVPE but not been removed can be etched away. Therefore, if the etching time is adjusted carefully, no additional material is removed from the substrate wafer. Therefore, the additional costs are not substantial.
Accounting for the differences in efficiency (29% for the GaAs thin-film and 15% of the InP nanowire array), and the factor of four in material costs of InP compared to GaAs wafers, we estimate a substrate cost of ~1.09 $/W for MOVPE and CSVT InP nanowires. For GaAs thin-films (~29%) and GaAs nanowires (~29%), either grown by SA-MOVPE or CSVT, the costs are ~0.16 $/W. The costs for the top-down etching approach are discussed in growth section 6.4.2.

**Chemical vs. mechanical peel-off**

The mechanical lift-off step does not contain material but only depreciation, labor and maintenance costs associated with the equipment. The mechanical lift-off tool would be similar in terms of mechanics than the lift-off tool for the GaAs thin-films, however without chemical baths and much faster process speed. Therefore, we assume the same costs for the equipment, adjusted for the initially lower efficiency of the first generation of InP nanowire solar cells.

**Contacts**

The costs for the back side and front side metalization are the same for GaAs thin-film solar cells and the nanowire solar cells and only need to be adjusted for the different efficiencies.[175] In the case of the nanowires solar cells, additional costs occur because of the need for a TCO on the front side. The material and deposition costs for a standard TCO amount to about 10 $/m², which translates to about 0.05 $/W for a 20% efficient solar cell.[202]

In the costs for the contacts we also included the costs of the MOVPE growth of the doped regions, contacting and buffer layers for the front and the back contacts. Those amount to 0.16 $/W and 0.25 $/W for the thin-film, respectively. For the nanowires we only included the growth of the BSF and emitter steps which amounts to in total 0.2 $/W for the 15% GaAs nanowire array (and respectively for the other efficiencies). For the GaAs thin-films additional costs arise due to the contact layer etch step, that is 0.06 $/W. In total the contacting costs for the GaAs thin-film solar cells amount to about 0.67 $/W and to 0.52 $/W for the 15% GaAs nanowire solar cells (and respectively for the other efficiencies). We assumed roughly the same costs for back and front side metalization for GaAs thin-films (compared to [175]).

The MOVPE contacting steps would have to be replaced for CSVT or top-down etching. For both, CSVT and top-down etching we assume the contacting costs to be essentially determined by the ITO deposition and metalization, in total 0.34 $/W ($ =15%) for both sides. The growth steps of the doped layers are negligible for CSVT, because the growth of the main absorber is already very low. The profound cost difference of the technologies occurs because of the absorber growth steps, as shown in Fig. 6.8 (and the substrate for InP nanowires).