The building block method. Component-based architectural design for large software-intensive product families
Müller, J.K.

Citation for published version (APA):

General rights
It is not permitted to download or to forward/distribute the text or part of it without the consent of the author(s) and/or copyright holder(s), other than for strictly personal, individual use, unless the work is under an open content license (like Creative Commons).

Disclaimer/Complaints regulations
If you believe that digital publication of certain material infringes any of your rights or (privacy) interests, please let the Library know, stating your reasons. In case of a legitimate complaint, the Library will make the material inaccessible and/or remove it from the website. Please Ask the Library: http://uba.uva.nl/en/contact, or a letter to: Library of the University of Amsterdam, Secretariat, Singel 425, 1012 WP Amsterdam, The Netherlands. You will be contacted as soon as possible.
List of Figures

Figure 1: System Theory: A System .............................................. 7
Figure 2: System of Interest and Application Domain ...................... 9
Figure 3: System Functionality Origins ....................................... 9
Figure 4: Model for Architecting ............................................... 14
Figure 5: Application Domain Modelling ..................................... 16
Figure 6: Feature-Centric Transition .......................................... 20
Figure 7: Feature Matrices ....................................................... 20
Figure 8: Base Products and Features ........................................ 21
Figure 9: BBM: Input - Output Specification ................................ 24
Figure 10: Dependent Functional Block Structure .......................... 27
Figure 11: Independent Functional Block Structure ......................... 28
Figure 12: Feature-Oriented Application Structure .......................... 28
Figure 13: Concepts of the BBM and their Main Relations ................. 29
Figure 14: Prerequisites for the BBM ......................................... 32
Figure 15: Main Design Tasks ..................................................... 33
Figure 16: Aspects and Domain-Induced Objects ............................ 35
Figure 17: Thread Identification ............................................... 35
Figure 18: BB and Objects ....................................................... 36
Figure 19: Mapping of Objects, Aspects and Threads to BBs ............... 37
Figure 20: Dependency Relation Between BBs ............................... 37
Figure 21: Identification of Deployment Sets .................................. 39
Figure 22: Input + Output of Design Tasks ................................... 40
Figure 23: Three Design Dimensions ........................................... 45
Figure 24: Mapping of Domain Model to Software .......................... 56
Figure 25: Examples of Sources of Objects ................................... 59
Figure 26: Initial Two Layers .................................................... 60
Figure 27: Three Layers with Basic and Advanced Applications ........... 61
Figure 28: Four Layers with Operating Infrastructure ....................... 61
Figure 29: tss Layered Subsystems .............................................. 64
Figure 30: Architectural Concern Analysis .................................... 73
Figure 31: Examples of SW Aspect Stimuli .................................... 78
Figure 32: Aspect Structuring of Building Blocks ............................ 82
Figure 33: Multi-View Approaches ............................................. 85
List of Figures

Figure 34: Requires and Provides Interfaces .................................................. 100
Figure 35: Abstraction and Open Implementation Interfaces ............................ 101
Figure 36: Call Back Mechanism ..................................................................... 102
Figure 37: User vs. HW Technology Layering .................................................. 105
Figure 38: Abstraction from HW ................................................................. 106
Figure 39: Generic vs. Specific ........................................................................ 106
Figure 40: Partial Layering ............................................................................. 110
Figure 41: Indirect Peer-to-Peer Communication ............................................. 111
Figure 42: Generic BB and Specific BBs .......................................................... 114
Figure 43: Generic and Specifics with Interfaces .............................................. 116
Figure 44: Abstraction Generic ........................................................................ 117
Figure 45: Connectable Resource Generic and Resource Flow ......................... 118
Figure 46: System Infrastructure Generics ....................................................... 120
Figure 47: Layer Access Generic ..................................................................... 122
Figure 48: System Structure with HW Mirroring in EM .................................... 124
Figure 49: BBM Interfaces .............................................................................. 125
Figure 50: Architectural Skeleton ..................................................................... 127
Figure 51: Basic Pattern for Diversity ............................................................. 140
Figure 52: Regular Layered Diversity ............................................................... 141
Figure 53: Feature Relation and BB Relation ................................................... 144
Figure 54: Application Feature Implementation Relation .................................. 145
Figure 55: Peripheral Card Maintenance ......................................................... 146
Figure 56: Soni’s Architectural Model .............................................................. 158
Figure 57: 4+1 Architectural Model ................................................................. 159
Figure 58: Tree-Type Control Structure ........................................................... 165
Figure 59: Three Stage Control Communication Structuring ............................. 166
Figure 60: Connection Structure of a Central Controller .................................. 168
Figure 61: Managed Object ............................................................................ 169
Figure 62: Mapping of External Objects to Internal Objects ............................. 170
Figure 63: The Basic Two Layers .................................................................... 171
Figure 64: Three Layers .................................................................................. 172
Figure 65: Four Layers with Multi-site Resources .......................................... 172
Figure 66: Four Layers with Basic and Advanced Applications ....................... 173
Figure 67: Four Layers with Operating Infrastructure ....................................... 173
Figure 68: Control spheres of EM .................................................................... 174
Figure 69: Communication Relations of EM .................................................... 174
Figure 70: Relations between CM,FM and PM ............................................... 177
Figure 71: Documentation Dependencies ....................................................... 185
Figure 72: Layered Processes .......................................................................... 186
Figure 73: DDD and Generators ...................................................................... 188
Figure 74: The Architect’s Depth of Understanding ......................................... 189
List of Figures

Figure 75: Switching Systems in Context ........................................... 196
Figure 76: tss Hardware Architecture ............................................... 198
Figure 77: Three Peripheral Groups ................................................ 199
Figure 78: Layered Subsystems ..................................................... 201
Figure 79: Peer-To-Peer Communication .......................................... 202
Figure 80: Mapping of Objects to Layers .......................................... 203
Figure 81: tss State Model ............................................................. 209
Figure 82: Recovery Phase Hierarchy ................................................ 213
Figure 83: tss Addressing Scheme .................................................. 218
Figure 84: Service Interface of a BB descriptor .................................. 219
Figure 85: Call-back Registration .................................................... 220
Figure 86: Recovery Interface of the BB descriptor ................................ 221
Figure 87: Generic and Specifics with Interfaces ................................ 222
Figure 88: System Infrastructure Generics ......................................... 223
Figure 89: Connectable Resource Generic and Resource Flow ............... 225
Figure 90: Layer Access Generics ................................................... 227
Figure 91: Tree-Type Control Structure ............................................ 229
Figure 92: System Structure with HW Mirroring in EM ..................... 230
Figure 93: Evolving the Construction Set ......................................... 243
Figure 94: Development Steps to Extend the Construction Set ............. 244
Figure 95: Overview of the DDD ..................................................... 245
Figure 96: Process Steps for Configuring a Product Instance ................ 247
Figure 97: Process Overview of Product and Site Configuration ............ 248
Figure 98: Construction Sets and Projects ........................................ 256
Figure 99: Empirical Data on the Distribution of Efforts ...................... 260
List of Figures