The ATLAS SemiConductor Tracker Endcap
Peeters, S.J.M.

Citation for published version (APA):

General rights
It is not permitted to download or to forward/distribute the text or part of it without the consent of the author(s) and/or copyright holder(s), other than for strictly personal, individual use, unless the work is under an open content license (like Creative Commons).

Disclaimer/Complaints regulations
If you believe that digital publication of certain material infringes any of your rights or (privacy) interests, please let the Library know, stating your reasons. In case of a legitimate complaint, the Library will make the material inaccessible and/or remove it from the website. Please Ask the Library: http://uba.uva.nl/en/contact, or a letter to: Library of the University of Amsterdam, Secretariat, Singel 425, 1012 WP Amsterdam, The Netherlands. You will be contacted as soon as possible.
Chapter 3

The SCT end-cap detector

"Any sufficiently advanced technology is indistinguishable from magic."

Arthur C. Clarke

Figure 3.1: The relative position of the silicon strip sensors of the ATLAS SemiConductor Tracker endcap. The endcap is approximately 2 m long and 1.2 m in diameter.
Figure 3.1 shows the layout of the active silicon in one End-cap of the ATLAS Semiconductor Tracker. The total silicon area for one End-cap is 6.21 m$^2$, which is divided over 988 modules. Since each module reads out 1536 channels, this represents just over 1.5 x 10$^6$ silicon strips that are expected to have a maximum occupancy of 1% and are to be read-out at an average frequency of 100 kHz.

This chapter gives a description of the end-cap design, focused on the technology choices made to meet the challenging requirements stated above, using as little material as possible in order not to distort the tracks and the energy of the particles. In addition, once the detector is installed in ATLAS, it will be very hard to access. Therefore, the detector has to be able to run without maintenance, preferably for the full expected ATLAS lifetime of ten years. The chapter starts with a description of the detector layout. The next section gives an overview of the mechanical support and the services. Then the detector modules are described in detail.

3.1 Layout

A disc is fully covered with silicon in three rings. The modules of the inner and outer rings sit on one side of a support disc, and putting a ring of middle modules on the other side fills the radial gap. The modules are mounted on cooling blocks that come in two heights, allowing adjacent modules in a ring to overlap. The nine discs of one end-cap are positioned so to that most straight tracks give at least four hits (Haywood 2002a).

The modules consist of single-sided silicon-strip sensors, glued back-to-back on a ‘Thermal Pyroilic Graphite’ (TPG) spine, with a small stereo angle (40 mrad, i.e. about 2.3°). The silicon

![Diagram of the layout parameters of the forward SCT.](image)

Table 3.1: The main layout parameters of the forward SCT. The z-coordinate refers to the centre of the disc. The module centre is offset 12.5 or 18.7 mm from this, depending on whether the module is mounted on a low or high cooling block. The inner and outer modules are mounted on the low-z side of the disc, the middle modules on the high-z side. The orientation parameters are illustrated in the drawing on the left. The modules are viewed from the interaction point. The exact definition is given in the text. The order of the orientation parameter is as a particle coming from the interaction point will meet them. * indicates middle modules of half-length. ** indicates outer modules sitting on the high-z side of the disc (the disc is manufactured as a φ-v disc and then rotated, becoming U-φ).

<table>
<thead>
<tr>
<th>wheel nr.</th>
<th>z (mm)</th>
<th>orientation</th>
<th>inner</th>
<th>middle</th>
<th>outer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>852.8</td>
<td>U-φ</td>
<td>-</td>
<td>40</td>
<td>52</td>
</tr>
<tr>
<td>2</td>
<td>931.6</td>
<td>φ-v</td>
<td>40</td>
<td>40</td>
<td>52</td>
</tr>
<tr>
<td>3</td>
<td>1092.2</td>
<td>U-φ</td>
<td>40</td>
<td>40</td>
<td>52</td>
</tr>
<tr>
<td>4</td>
<td>1300.6</td>
<td>φ-v</td>
<td>40</td>
<td>40</td>
<td>52</td>
</tr>
<tr>
<td>5</td>
<td>1401.4</td>
<td>U-φ</td>
<td>40</td>
<td>40</td>
<td>52</td>
</tr>
<tr>
<td>6</td>
<td>1772.9</td>
<td>φ-v</td>
<td>40</td>
<td>40</td>
<td>52</td>
</tr>
<tr>
<td>7</td>
<td>2114.7</td>
<td>U-φ</td>
<td>-</td>
<td>40*</td>
<td>52</td>
</tr>
<tr>
<td>8</td>
<td>2504.6</td>
<td>φ-v</td>
<td>-</td>
<td>52</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>2719.8</td>
<td>U-φ</td>
<td>-</td>
<td>-</td>
<td>52**</td>
</tr>
</tbody>
</table>
sensors are wedge-shaped. The modules are placed on the discs such that one side has its strip in the radial direction of the ATLAS coordinate-system, the so-called $\phi$-orientation. The other side of the module has its strip in either the $u$ or the $v$-direction. These are defined as (Haywood 2002b):

- When viewing the end-cap from the interaction point, the $u$-strips are obtained from the $\phi$-strips by a clockwise rotation by the stereo angle about an axis parallel to the B-field.

- When viewing the end-cap from the interaction point, the $v$-strips are obtained from the $\phi$-strips by an anti-clockwise rotation by the stereo angle about an axis parallel to the B-field.

Note that the end-caps are manufactured to be identical.

Table 3.1 gives more quantitative layout information. The drawing next to the table shows modules as seen from the interaction point, and indicates the orientations. Section 3.3.2.3 gives more details on the sensors; Table 3.4 shows the main parameters. This layout has an $\eta$-coverage from 1.4 to almost 2.5.

### 3.2 Peripherals

![Figure 3.2: An impression of the end-cap SCT services, surrounding the disks holding the detector modules. The interaction point of the LHC beams is on the left.](image)
The SCT end-cap detector

Many services are required to mechanically hold, cool, power and align the detector. Figure 3.2 shows an overview of the total end-cap. This section briefly describes the components of an end-cap, other than the detector modules. More details can be found in (ATLAS Inner Detector Collaboration 1997a, ATLAS Inner Detector Collaboration 1997b).

3.2.1 Radiation length

One of the main requirements of every item in the end-cap, is a low radiation length. The radiation length $X_0$ of a material is the mean distance over which a high-energy electron loses all but $1/e$ of its energy by Bremsstrahlung. For electrons this is the dominant energy-loss process for energies higher than the critical energy $E_c$, which can be approximated by (Hagiwara et al. 2002):

$$E_c = \frac{610}{Z + 1.24} \text{ MeV}$$

where $Z$ is the atomic number of the material. From this equation it can be seen that for most materials and an electron energy of more than 1 GeV, Bremsstrahlung by far dominates the energy-loss.

The radiation length can be calculated to reasonable accuracy ($< 3\%$) for a pure-element material with atomic number $Z$, atomic weight $A$, and density $\rho$ (in g/cm$^3$) from (Hagiwara et al. 2002):

$$X_0 = \frac{7164 A}{Z(Z + 1)\rho \ln (287/\sqrt{Z})} \text{ (mm)}$$

This equation clearly shows that the use of elements with a low $Z$ is preferred. The radiation length in a mixture or compound can be approximated by:

$$\frac{1}{X_0} = \sum_j \frac{1}{X_j}$$

where $X_j$ is the radiation length of an element, using its partial density for $\rho$ in Equation 3.2. Table 3.2 gives the radiation length of many of the materials used in the SCT. In traversing a material over a distance $t$, the percentage of radiation length traversed is:

$$\%X_0 = \frac{t}{X_0} \times 100\%$$

This quantity is very useful because it is additive over different materials along a particle track.

<table>
<thead>
<tr>
<th>material</th>
<th>$X_0$ (mm)</th>
<th>comment</th>
<th>material</th>
<th>$X_0$ (mm)</th>
<th>comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>graphite</td>
<td>189</td>
<td>pure</td>
<td>silicon</td>
<td>93.6</td>
<td></td>
</tr>
<tr>
<td>TPG</td>
<td>200</td>
<td></td>
<td>Korex</td>
<td>$13 \times 10^3$</td>
<td>typical</td>
</tr>
<tr>
<td>Carbon-Carbon</td>
<td>220</td>
<td></td>
<td>plastics</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>carbon-fibre skin</td>
<td>250</td>
<td></td>
<td>Al</td>
<td>89</td>
<td></td>
</tr>
<tr>
<td>Kapton (polyimide)</td>
<td>350</td>
<td></td>
<td>stainless steel</td>
<td>18.0</td>
<td></td>
</tr>
<tr>
<td>$C_3F_8$</td>
<td>$1.8 \times 10^3$</td>
<td>gas, -20 °C, 2 bar</td>
<td>Cu</td>
<td>14.35</td>
<td>pure</td>
</tr>
<tr>
<td>$C_3F_8$</td>
<td>225</td>
<td></td>
<td>Cu-Ni</td>
<td>14.4</td>
<td></td>
</tr>
<tr>
<td>$N_2$</td>
<td>$47 \times 10^3$</td>
<td>20 °C, 1 bar</td>
<td>solder</td>
<td>8.8</td>
<td>Sn-Pb</td>
</tr>
</tbody>
</table>

Table 3.2: The radiation length of some of the materials used in the SCT.
3.2.2 Support structure

The purpose of the support structure (see Figure 3.3) is to hold the silicon detector sensors in the correct place with a high degree of stability. Some movement can be tolerated, as long as it is slow enough to be measured using tracks, which is the most precise method to measure detector positions in a running experiment. The detectors should move significantly less than the hit resolution (23 μm) within the time needed to make a track alignment. In 24 hours enough tracks will be recorded to carry out a software alignment with a precision of about 1 μm (Peeters 1999). The system should also not vibrate. Stability requires stiff, light-weight materials that are not sensitive to changes in the environment: radiation, temperature and moisture. The support structure should also have low radiation-length. Carbon-fibre meets all of these requirements.

The cylinder is a sandwich of carbon-fibre, honeycomb and carbon-fibre, which makes a very stiff composite (Tarrant et al. 2002). The cylinder is supported by two wings, suspended at four points on the squirrel cage rails which are attached to the solenoid magnet. Although this over-constrains the end-cap, the movement of the four support points should be very small, so the internal distortion should be very small.

The cylinder holds nine support discs, made out of a similar sandwich as the cylinder. These discs hold the modules. They mount into the cylinder by specially designed springs (Hover 2001). The mountings ensure a stiff clamping of the disc onto the cylinder, keeping the eigen-frequencies of the disc above 20 Hz (Snippe 2001), while allowing expansion or contraction of a disc due to thermal and moisture changes without exerting large forces on the cylinder.

The specified stability of modules over 24 hours is 12 μm in the rφ-direction, 50 μm in the φ-direction and 200 μm in the z-direction.

Figure 3.3: The SCT end-cap support cylinder. The interaction point is on the right.


The expected maximum power-consumption for a module is 8 W (approximately 7 W in the electronics hybrid and 1 W in the silicon); so an end-cap produces approximately 8 kW of heat. This has to be removed by cooling. Furthermore, the silicon wafers have to be kept below −7 °C, both to minimise the effects of radiation damage (see Section 3.3.2.2) and to avoid thermal run-away. The power dissipated in the sensors makes the temperature increase, causing the sensor current to increase until the device is in thermal equilibrium with the heat removal system. If the current becomes too high, the module cooling can become inadequate and the current increases exponentially. The cooling system should be adequate to avoid thermal run-away below a sensor power-density of 240 W/m² (Snow 2001).

Figure 3.4 shows the principle of the cooling of a single detector module (the layout of a module is described in Section 3.3). The module is mounted on the disk onto two Carbon-Carbon blocks, which are also used for the cooling. These cooling blocks are connected to the cooling pipes, which transports the medium providing the cooling. One cooling block cools the electronics and the sensors, the other cooling block only cools the sensors. For the shortest module type (the so-called inner module), only the first cooling block is sufficient, therefore the other mounting point is not cooled.

The Carbon-Carbon has a very good heat conductivity in its two fibre directions and very low radiation length. This material has a heat conductivity of 300 Wm⁻¹K⁻¹ in two directions and 50 Wm⁻¹K⁻¹ in the other direction. One of the better conductive directions is aligned with the cooling pipes, to optimise the heat transfer. Also a insert made out of Peek is added to the further limit the flow from the electronics to the sensors. The radiation length of these blocks is low (see Table 3.2).

An evaporative cooling system has been chosen, with C₃F₈ as the coolant. This system is run in a bi-phase (liquid-gas) mode at an absolute pressure of 2 bar to achieve a high heat-transfer coefficient. The typical operation temperature of the cooling fluid is −20 °C, ensuring a sensor temperature below −7 °C. This system has been chosen for its low radiation-length, high heat-transfer coefficient (4 kW m⁻² K⁻¹) and relatively low temperature-drop along a cooling pipe. The expected cooling-block top surface temperature is −10 °C, which according to simulations should give a 3 °C hybrid temperature and an average chip-temperature of 8 °C (Snow 2001).

Since the cooling circuit contributes significantly to the total material budget of the end-cap, the heat-transfer coefficient is an important parameter in the cooling. If this is large, cooling

---

1This material is made out of carbon-fibre, of which the resin holding the fibres together is also carbonised.
pipes with a smaller diameter and hence less material can be used. The cooling pipes used for the SCT end-caps are made of a copper-nickel alloy and have a wall thickness of 70 µm. The pipe wall-thickness is not determined by pressure requirements anymore, but by the requirement that the cooling pipes can be bent and handled safely. Copper-nickel was chosen for its corrosion resistance and the ease with which it can be soldered.

The cooling pipes will not run circumferentially (see Figure 3.5), but will wiggle around a circumferential line (Temple 2001). The wiggles absorb the thermal expansion without forcing the cooling blocks to move. Therefore the cooling blocks can be glued on most points onto the disk, and only at some points the blocks need to be mounted on an aluminium insert in the disk, saving material. Figure 3.5 gives an impression of the cooling circuit for one quarter a disk.

### 3.2.4 Power cables

The power cables (Pernegger et al. 2001) connect control voltages and bias lines, which draw very little current, and connect the two power supplies: the analogue power supply $V_{cc}$ supplies 3.5 V to the module and draws approximately 0.9 A; and the digital power supply $V_{dd}$ supplies 4.0 V and draws approximately 0.6 A. They should be of low mass and take up as little volume as possible. The voltage drop on the power cables should be low to avoid costly power-supplies, conflicting with the low-mass requirement.
This conflict is handled by splitting the cabling up in five parts, see Figure 3.6. In the places where the radiation length is most crucial very low mass cables are used, in the other places, more material is added to minimise the voltage drop. The expected voltage drop for this configuration is 2.4 V for $V_{dd}$ and 3.5 V for $V_{cc}$, including the return and assuming the currents as stated before.

The power supplies will be situated in side caverns near ATLAS (half in US15 and half in USA15). One power cable per module goes to the ATLAS cavern. This cable starts with type IV, a conventional thick cable to achieve as little voltage-drop as possible. It is connected to a thinner conventional cable (type III) via patch-panel 3 (PP3) in the ATLAS cavern. PP3 is outside the magnetic fields of ATLAS and it uses inductors with magnetic cores to filter all lines. The cable type III continues to the crack between the barrel and end-cap calorimeter in ATLAS. Here a cable-to-cable connection (this used to be PP2) is made to an even thinner conventional cable (type II), which is continued to the end of the cryostat bore. Here it is connected to patch-panel PPF1 (F for forward). This patch-panel adds filters to all lines and connects a ‘low-mass’ tape (type I): a double lamination of aluminium-Kapton. On the edge of the disc, the low-mass tape is connected to patch-panel PPF0. From here the module is connected using ‘low-low-mass’ tape, made of a double lamination of copper-Kapton for the control lines and bias lines, and copper or aluminium twisted pairs for $V_{cc}$ and $V_{dd}$.

The patch-panel PP3 has voltage-limiters for the $V_{dd}$ and $V_{cc}$ that are sensed on the module. This protects the module from a too high voltage-bias in case of a failure of the sense-wires. This patch-panel also incorporates filtering on all the lines. The patch-panel PPF1 filters the $V_{dd}$-lines, $V_{cc}$-lines, their sense-lines, and the sensor-bias lines. The patch-panel PPF0 has no filtering.

### 3.2.5 Control and read-out fibres

The optical fibres fulfil the low-mass requirement and take little space. The fibres used are radiation hard (Mahout et al. 2001). The routing should be carefully designed, due to the limited bending radius of the fibres: if the fibres are bent too much, they leak light. The light used (840 nm) has a quantum-efficiency of 100% to create an electron-hole pair in silicon. Therefore, the fibres are clad in black plastic.
3.2.6 Thermal shield

To ensure absolute thermal neutrality of the SCT end-cap within the ATLAS detector, it will be enclosed in an active thermal shield (Tarrant et al. 2001). This has a heater on the outside, followed by an insulator, and then a cooler on the inside. The heater provides the heat-flux through the insulator necessary to maintain the temperature drop from the outside to the inside. The cooler removes this heat, to avoid extra heat load on the sensors.

Kapton foils with aluminium traces are used as heaters. Thin aluminium pipes, flushed with C₆F₁₆ cooling fluid provide the cooling. Structural foam (Airex R82), which has a thermal conductivity of only 40·10⁻³ W m⁻¹ K⁻¹, is used for the insulator. The radiation length contribution of this system is only 0.41% for tracks which traverse the material at a perpendicular angle. However, due to the cylindrical shape of the system, this becomes significant at large $\eta$.

3.2.7 FSI alignment system

The hardware alignment system implemented is a frequency scanning interferometer (Howell et al. 2002). This method allows the changes in the 3-dimensional position of the discs to be determined with a precision of $\lesssim 10 \mu m$. This is significantly worse than should be achievable with tracks (ATLAS Collaboration 1999a), but it measures the disc position on a short time-scale (minutes) compared to tracks (hours), allowing short term movements to be observed. Coupled with the X-ray survey mentioned below, it can give the initial wheel positions after installation. The software analysis of tracking data has been proven to take a long time to get operational for existing experiments, hence this alignment system should allow a better initial understanding of the end-cap and thus effectively a quicker start-up of the experiment.

The FSI-system uses scanning of the frequencies, which allows the interferometer to be turned on and off and still measure an absolute length. It uses a large number of measurements to recover the end-cap geometry. For every measurement a single-mode input fibre, a retro-reflector (an aluminium cube-corner) and a single-mode output-fibre needs to be installed. These components are radiation hard and add only a small amount of material.

Before the installation of the end-cap in ATLAS, the entire SCT will be surveyed by X-ray while running the FSI system, the modules and the cooling: in addition to measuring the module positions, this calibrates the FSI-system.

3.2.8 Other peripherals

The end-caps will also be equipped with magnetic field sensors, radiation monitors, humidity sensors, and temperature sensors. The design of these still has to be clarified, however, these items will be small and amount to little radiation length. They will be read out by the Detector Control System (DCS).

3.3 Detector modules

Figure 3.7 shows the three SCT end-cap detector modules. This section describes in detail the design and the technology of the inner module, which is the module type to be built at NIKHEF.
The inner module holds two sensors, while the outer and middle module consist of two pairs of sensors on each side of the detector, with interconnected strips\(^2\).

### 3.3.1 Module design

Figure 3.8 shows the individual components of an end-cap module. Figure 3.9 shows a photo of an end-cap module. The sensors are glued back-to-back onto a spine. This spine also electrically connects the sensor backplanes and the bias voltage, and transports the thermal power generated in the sensors to the cooling blocks. The central part of the spine is made of ‘Thermal Pyrolytic Graphite’ (TPG), graphite made at high temperatures and pressures, which ensures a close to perfect crystal structure. The thermal conductivity in the plane of the graphite crystal structure is approximately 1100 WK\(^{-1}\)m\(^{-1}\). The TPG is encapsulated in Parylene to avoid moisture absorption. The crossbars of the spine are made out of aluminium-nitride (AlN), and can be used to pick up the module by hand.

Two washers made out of glass fibre with an aluminium precision insert determine the position of the sensors on the discs. These washers are glued onto the spine.

The sensors are read-out with an electronics hybrid, which holds twelve read-out chips

\(^2\)At the time of design of the sensors, the most common wafer size in industry was four inch. This has driven the dimensions of the modules. At the time of writing this thesis, six inch wafers are commonly used in industry.
3.3. Detector modules

Figure 3.8: Exploded view of an end-cap inner detector module, showing (a selection of) the individual components

(ABCD) and two chips (VDC and DORIC) controlling the optical link. Each ABCD chip reads out 128 channels and for each channel it amplifies and shapes the signal, after which it is compared to a threshold. After this the signal is binary: if the signal is above threshold, a ‘1’ is registered, otherwise a ‘0’. This information is stored in a pipeline and upon receipt of a LVL1 trigger (see Section 2.2.6), this information is read-out. The chips are described in more detail later in this section. The electronics hybrid holds the chips and passive components and is made out of a four-layer Kapton-copper structure, which is folded around a Carbon-Carbon baseplate. The hybrid is discussed in detail in Chapter 7. The connection between the sensors and the chips is made via four glass fan-ins with aluminium traces.

The sensor bias is supplied via a conductive line that is printed onto the AIN-part of the spine, on the hybrid-side. This line connects the hybrid high-voltage line to the sensor backplane, on both sides of the module. Both sides are interconnected via a plated hole in the AIN. For outer and middle modules, the two sensors on the far-side from the hybrid are connected to the sensor bias using similar traces on the middle AIN-part of the spine (see Figure 3.7). These traces connect both backplanes of the two sensors on one side of the module. To make sure that the TPG does not induce any noise via pick-up, it is connected using conducting glue to the backplane of one of the sensors, via a gap in the Parylene coating.
3.3.2 Silicon

3.3.2.1 Silicon as a particle detection medium

There are several advantages of using silicon as a detection medium for charged particles (Lutz 1999):

- The high mobility of the charge carriers enables fast charge collection times (approximately 5 ns for electrons, the charge creation time can be neglected).

- The high density of silicon in combination with the relatively low energy needed to create an electron-hole pair (equivalent to 3.6 eV, compared to the (typically) 30 eV needed for single ionisation in a gaseous medium) renders it possible to make very thin detectors which still produce a reasonable signal.

Table 3.3 gives an overview of the most important properties of silicon relevant to this thesis.

To enable a fast charge-collection, a voltage needs to be applied across the silicon sensor. To prevent this producing a large current, silicon sensors use ‘pn-junctions’ which form diodes
3.3. Detector modules

and are operated with a reverse bias. The elementary principles of silicon diodes are explained in the remainder of this paragraph, more details can be found in (Sze 1985).

The energy levels of the electrons in a semiconductor can be represented in two bands: a conduction band and a valence band. These two bands are separated by a forbidden region, the ‘band-gap’. Electrons in the lower energy band, the valence band, form the inter-atom covalent bonds. If a bond breaks, an electron is moved to the conduction band, where it is free to participate in current conduction. The transition of an electron from the valence band to the conduction band can be caused by absorption of energy. This energy can be provided thermally or by a particle traversing the silicon. The electron deficiency that is left in the covalent bond may be filled by one of the neighbouring electrons, resulting in a shift of the deficiency location. This mobile deficiency location can be treated as a particle and is called a ‘hole’.

In pure silicon, the number of holes and conduction electrons is exactly equal. To alter the properties of the silicon, impurities are added (doping). Silicon itself has four valence electrons. Addition of matter with five valence-electrons makes n-type (‘negative carriers’) silicon: conduction is mostly due to electrons. Addition of matter with three valence-electrons makes p-type (‘positive carrier’) silicon. In this electrically neutral material holes dominate the conduction.

The bulk material of the SCT sensors is n-type. The diode is formed by implanting a thin layer of extra-highly doped p-type, so-called p⁺-type. Conduction electrons from the n-type diffuse to the p⁺-type and fill the holes and vice versa. The absorption of charge carriers in the originally electrically neutral materials leads to a build-up of charge, and thus a potential difference (generally referred to as $V_{bi}$) across the pn-junction. This potential difference counteracts further diffusion of electrons and holes, creating a region around the pn-junction in which the mobile charge-carrier density is zero. This region is called the ‘depletion region’ or ‘space-charge region’. This mechanism is illustrated in Figure 3.10 (a). This region can be enlarged by applying an external voltage in the same direction as $V_{bi}$. Using highly-resistive silicon ensures that the entire sensor can be depleted, well below the breakdown field of silicon (approximately $5 \times 10^5$ V/cm, i.e. approximately 14 kV for the SCT), with low leakage current.

The pn-junction can be used to make a position-sensitive detector, see Figure 3.10 (b). The $p^+$-type is implanted in strips on an n-type substrate (to achieve reverse bias, the backplane is put at a positive voltage with respect to the strips). The strips are surrounded by a guard ring structure at the edges, as shown, that is connected to the same potential as the backplane. This avoids potential difference along the edges of the sensor, and thus high leakage currents. The $n^+$-type layer is implanted on the backside, because the metal-semiconductor contact forms a Schottky

<table>
<thead>
<tr>
<th>property</th>
<th>value</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic weight</td>
<td>28.09</td>
<td></td>
</tr>
<tr>
<td>Density</td>
<td>$2.33 \times 10^{-3}$</td>
<td>kg/m³</td>
</tr>
<tr>
<td>Radiation length</td>
<td>93.6</td>
<td>mm</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Band gap (eV)</td>
<td>1.12</td>
<td>eV</td>
</tr>
<tr>
<td>Equivalent energy to create an electron-hole pair</td>
<td>3.6</td>
<td>eV</td>
</tr>
<tr>
<td>Logarithmic average ionisation-energy</td>
<td>174</td>
<td>eV</td>
</tr>
</tbody>
</table>

*Table 3.3: Some properties of silicon at room temperature.*
barrier (Sze 1985): a charge barrier similar to a \(pn\)-junction. Adding a highly-doped region of silicon to make the contact, reduces the width of the potential barrier, making the characteristic resistance of the formed junction very small.

A charged particle traversing the silicon ionises it, creating conduction electrons and holes, which drift to the electrodes inducing a current. This current is detected and, since it is associated to a strip, the position where the particle traversed the sensor is determined. The signal-generation process is described in Section 6.1.1.

### 3.3.2.2 Expected radiation dose and radiation hardness

The most challenging design requirement of the silicon sensors is the radiation hardness. This section first discusses the expected radiation dose and then the effects of radiation damage are discussed.

Two types of radiation are distinguished: ionising radiation, caused by charged particles, and non-ionising radiation, in principle caused by all particles, but in practice mainly by hadronic particles. The expected radiation dose in the SCT is \(1.3 \times 10^{13} \text{ 1 MeV neutron equivalent (n}_{\text{eq}})\) per cm\(^{-2}\) for one year of ATLAS at full luminosity\(^3\) (Dawson & Buttar 2000). This dose is mainly due to the charged particles produced in the LHC interaction and the neutron back-shine from the calorimeters. The latter becomes important in the Inner Detector close to the calorimeters; i.e. at large radii or large \(\eta\). This back shine is reduced at large \(\eta\) by shielding with polythene discs on the inside of the end-cap calorimeters. At large radii, the TRT radiator provides shielding for the SCT. After ten years of ATLAS a total integrated-dose of \(1.3 \times 10^{14} \text{n}_{\text{eq}} \text{ cm}^{-2}\) is expected. An uncertainty of 50\% is usually assumed to account for the uncertainties in total pp cross-section

---

\(^3\)This unit is common for silicon detectors. The integrated effect of the radiation damage is expressed as the number of 1 MeV neutrons needed to accomplish the same radiation damage.
and the neutron back shine of the calorimeters. A conservative estimate of the maximum expected radiation dose in the ATLAS SCT is then approximately $2 \times 10^{14} \text{n}_{\text{eq}} \text{cm}^{-2}$. The sensors are tested for radiation hardness at the CERN PS accelerator which supplies a high dose of 24 GeV protons. The sensors have to survive an integrated dose of approximately $3 \times 10^{14} \text{p cm}^{-2}$, which approximately corresponds to $2 \times 10^{14} \text{n}_{\text{eq}} \text{cm}^{-2}$.

The effects of non-ionising radiation are dislocation of atoms and nuclear reactions, introducing impurities in the lattice. This mainly causes bulk damage, that has three main effects: it creates traps for carriers, causing a reduction in charge collection and hence signal height and the timing of the signal; it reduces the band-gap, giving higher leakage currents; and it changes the effective doping of the silicon.

Ionising radiation creates mobile or trapped electron-hole pairs. Mobile electron-hole pairs provide the detection signal, but trapped pairs mainly cause surface and oxide damage. The charge build-up because of this damage increases the strip capacitance, giving higher noise and lower signal height. The interstrip capacitance is expected to increase about 20% over the life of the modules (RD20 Collaboration 1993). It also increases strip-to-strip signal differences.

The three main consequences of radiation are: an increase in the sensor (interstrip) capacitance; an increase in the leakage current; and an increased depletion voltage.

The reduction in charge collection can be avoided by applying a higher bias voltage. Some SCT sensors may require 450 V to be fully efficient after 10 years in ATLAS.

The main contribution to the leakage current is from the bulk volume rather than edge or surface effects. In the absence of annealing, this bulk current density $I_b$ increases linearly with radiation fluence $\phi$ from its unirradiated level $I_0$:

$$I_b = I_0 + \alpha \phi$$  \hspace{1cm} (3.5)

The change in effective doping $N_{\text{eff}}$ of the bulk silicon alters the depletion voltage $V_{\text{dep}}$ (Pitzl
Figure 3.12: The left plot shows the depletion voltage as function of time for SCT sensors. The right plots shows the depletion voltage after ten years of operation at ATLAS as function of operating temperature.

\[ V_{\text{dep}} \approx \frac{q_0}{2e} |N_{\text{eff}}| t^2 \]  

where \( q_0 \) is the electron charge, \( e \) is the dielectric constant, and \( t \) is the silicon thickness. \( N_{\text{eff}} \) is the difference in donor and acceptor impurity concentration, \( N_D - N_A \) which is initially positive for the \( n \)-type bulk.

Dislocations mostly act as \( p \)-type dopant, either by compensating donors or by creating acceptors. The latter dominate, and are called deep-level acceptors, with energy level near the middle of the band-gap. They decrease the effective doping with radiation fluence \( \phi \):

\[ N_{\text{eff}}(\phi) = N_{D,0}e^{-\phi\epsilon} - N_{A,0} - \beta \phi \]  

where \( N_{D,0} \) and \( N_{A,0} \) are the initial donor and acceptor concentrations, \( \epsilon \) has the dimensions of area and can be interpreted as the donor removal cross-section, and \( \beta \) represents the probability to create an acceptor state by a hadron per unit path length. Figure 3.11 shows the result of fits to data for a particular design of silicon sensors: the \( n \)-type bulk eventually becomes \( p \)-type, called type-inversion (Wunstorf 1992).

After type-inversion, the diode junction moves from the strip-side of the silicon to the \( n^+p \)-junction at the reverse side. From Equation 3.6, after a certain dose \( V_{\text{dep}} \) starts rising above its initial value; SCT sensors are expected to require a depletion voltage of 350 V when fully irradiated.

The dislocations can change with time, even in the absence of irradiation, especially at higher temperatures. Dislocated atoms can be thermally vibrated back into the lattice, in a process known as ‘beneficial annealing’. This reduces \( |N_{\text{eff}}| \) and hence the depletion voltage and leakage current. It is a relatively rapid process, with a typical time constant of two weeks.
3.3. Detector modules

A slower process also occurs, known as 'reverse annealing' which increases $|N_{\text{eff}}|$, so that after an initial time of improvement from beneficial annealing, $V_{\text{dep}}$ and $I_b$ start increasing again. This is less well understood, but seems to be due to diffusion of dislocations or (induced) impurities and the formation of deep acceptors. Both processes are very slow at 0 °C, and stops at approximately $-10$ °C (Matthews et al. 1996). The SCT sensors will be kept below $-7$ °C cold once irradiated, except for maintenance. The effect of a possible scenario is shown in Figure 3.12. The left figure, from (ATLAS Inner Detector Collaboration 1997b), clearly illustrates the drastic effects of warm-up. The right figure, also from (ATLAS Inner Detector Collaboration 1997b), shows the temperature dependence of the expected depletion voltage after ten years of ATLAS. It illustrates the small dependence of the depletion voltage at the end of the last run-period on the temperature in the region between $-5$ °C and $-10$ °C.

3.3.2.3 Design

A lot of different designs of the sensors have been considered. For example, instead of single-sided $p$-strips in $n$-bulk two other options were considered: double-sided silicon sensors and sensors using $n^+$-strips on $n$-type bulk. To keep the costs down for the SCT, the most cost-efficient technology has been chosen.

The advantage of the first option is that instead of two sensors, only one is needed, inherently decreasing the radiation length. This decreases the radiation length of the SCT with an amount of 1.28%. The total radiation-length of the SCT is more than 20%. The yield of the sensors would be much lower due a much more complicated process, leading to significantly higher costs.

The advantage of using $n^+n$-sensors is that, after type inversion, the depletion region still starts from the strip side. Then, if for some reason the sensor cannot be fully depleted, the charge is more efficiently collected than for $p^+n$-sensors. Again, the expected yield for these sensors is lower, because they need a double-sided guard (Andricek et al. 2000). Also this technology needs $p$-stop implants in between the strips, which are not needed for $p^+n$-sensors. Finally, after irradiation the field gradient in the silicon is significantly higher than for $p^+n$-sensors.

The crystal orientation of the silicon chosen is $\langle 111 \rangle$ (the silicon crystal structure and its orientations are explained in for example (Lutz 1999)). In principle the orientation $\langle 001 \rangle$ could be better, since it has less dangling bonds at the surfaces which can be a source high surface leakage currents after irradiation (Demaria et al. 2000). For the ATLAS sensors both crystal orientations have been compared and no differences were found (Feld 2001b).

The inner modules sit in a higher radiation environment than others and thus need to be more radiation hard. The sensors of the inner modules that will be delivered to NIKHEF will be oxygenated, which enhances the radiation tolerance. It was found that after full irradiation, the required bias needed to reach full depletion was 80 V lower than for non-oxygenated sensors (Andricek et al. 2001).

Some parameters of the sensors are summarised in Table 3.4. Since the sensors have binary read-out, the resolution $\sigma$ can be calculated from the pitch $p$ from:
The SCT end-cap detector

\[
\sigma \equiv \sqrt{x^2 - \bar{x}^2} = \sqrt{\frac{1}{p} \int_{-\frac{1}{2}p}^{\frac{1}{2}p} x^2 dx} = \frac{p}{\sqrt{12}} \tag{3.8}
\]

3.3.3 Front-end Electronics

3.3.3.1 Overview

The SCT has opted for binary read-out of the strips, i.e. to know only that a strip had more than a certain level of charge generated in it, and not to know how much (analogue read-out). This simplifies the signal processing and reduces the amount of data to be read out. However, it complicates debugging the system, precludes making a coherent-noise correction, and limits the resolution to \( p/\sqrt{12} \), where \( p \) is the read-out pitch. The signals are processed in the so-called ABCD (A Binary Chip in DMILL-technology) front-end chips.

The analogue part of the ABCD first amplifies the small signals, then it shapes them for optimum signal-to-noise ratio within the constraint that two hits can be resolved provided they are separated by more than 50 ns. Finally the signal is discriminated, giving simply a ‘1’ if the signal is above a threshold and a ‘0’ otherwise.

This information is then transferred synchronously with each bunch crossing to the digital part of the electronics. There it has to be stored long enough for the first-level trigger to decide if it is wanted for further processing; this is the function of the pipeline memory. If wanted it is transferred to a buffer memory (‘derandomiser’), so that bunch crossings very close together in time can both be read out. From there, the data is compressed (zero-suppression) and sent to the read-out chip, the DORIC.

Optical links are used for communication to and from the module. This has two main advantages: the fibre optics have lower radiation length than copper wires; and the signals do not give or suffer from electro-magnetic interference. There are three components at the module: the opto-plugin which terminates the fibre optics and converts the optical commands to electrical signals and electrical data to optical for read-out; the DORIC (White 2002a) which decodes the incoming clock and commands and processes the outgoing data; and the VDC (White 2002b) (VCSEL driver chip) which provides the current for the VCSELs in the opto-plugin.

All this functionality is integrated on a single hybrid board (a hybrid of integrated circuit technology and surface mount component circuitry). This consists of a six-layer Kapton circuit

<table>
<thead>
<tr>
<th>module</th>
<th>wafers</th>
<th>radial pitch (( \mu )rad)</th>
<th>min. strip length (mm)</th>
<th>R centre (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>inner</td>
<td>W12</td>
<td>207.0</td>
<td>59.100</td>
<td>340.550</td>
</tr>
<tr>
<td>middle</td>
<td>W21</td>
<td>207.0</td>
<td>63.125</td>
<td>369.163</td>
</tr>
<tr>
<td></td>
<td>W22</td>
<td>207.0</td>
<td>52.475</td>
<td>429.063</td>
</tr>
<tr>
<td>outer</td>
<td>W31</td>
<td>161.5</td>
<td>63.850</td>
<td>470.555</td>
</tr>
<tr>
<td></td>
<td>W32</td>
<td>161.5</td>
<td>55.555</td>
<td>532.223</td>
</tr>
</tbody>
</table>

Table 3.4: The main parameters of the module sensors.
3.3. Detector modules

and holds 12 ABCD chips, one DORIC, and one VDC chip. It has a power connector, a connector for the opto-plugin and also ‘redundancy’ connectors: should the optical link of a module fail, it can either receive clock and command from a neighbour module or send its data via a neighbour, thus increasing the robustness of the system.

3.3.3.2 Technology

All three chips used in the module use the same, radiation hard technology: DMILL (Dentan et al. 1998). This electronics is based on 0.8 μm-technology VLSI (Very Large Scale Integration). The advantage of this technology is that it combines CMOS (Complementary Metal-Oxide-Semiconductor) with (analogue) PNP bipolar junction transistors (BJT), and can be implemented with radiation-hard capacitors and resistors. This allows analogue and digital circuits to be combined on one chip.

DMILL is radiation-hard up to 10 Mrad and \(10^{14}\) n\(_{eq}\). This is achieved by using a SOI (Silicon-On-Insulator) process. In this technology a thin silicon layer is created on top of an insulator. This top layer is then structured so that each transistor is built on its own island of silicon (Lutz 1999). This, together with insulated trenches, avoids unwanted currents, which ensures hardness for ionising radiation. The CMOS circuitry and BJT's are naturally radiation hard to neutrons. The complete insulation by the SOI and trenches minimise cross-talk effects via the substrate, allowing high-density integration of analogue and digital circuitry. An extra advantage of the CMOS technology is the relatively low power consumption.

3.3.3.3 The ABCD chip

Figure 3.13 shows an overview of the design of the ABCD chip up to the pipeline memory. This part will be discussed in more detail throughout this thesis. The part from the pipeline on consists of only digital functionality and is summarised at the end of this section.

The first part of the ABCD chip consists of a charge-sensitive amplifier and a shaper. The amplifier collector current and the shaper bias-current are set to one value for all channels. The design is such that the performance is not very dependent on the exact setting of these two currents. The default values used are 220 μA and 30 μA, respectively. Chapter 6 gives further details.

The signal is then digitised using a comparator, which compares the signal to a threshold. The overall threshold is set by a DAC (Digital to Analogue Converter) for the whole chip. Threshold correction circuitry compensates for channel-to-channel variations. This 4-bit trimming was implemented in the second prototype of this chip but turned out to have insufficient range to compensate the channel-to-channel variations after irradiation. Finally this was corrected by adding a 2-bit trim-range setting circuit, which alters the step size of the trim-setting.

The signal is fed through another comparator, to make the transition from the analogue to the digital power supply of the chip and is then amplified by three CMOS inverters to a level sufficient to drive the input register.

The signal is then fed into the input register, which latches it on one of the clock-edges. The signal is now fully digital and synchronised to the 40 MHz clock. The chip can be operated in either pulse or edge mode. In pulse mode, the signal in all time bins is latched, irrespective of the value in the preceding time bin. In edge mode, a hit is only latched if the preceding time bin
had no hit. After this a mask is applied: each individual channel can be switched off, useful if for example a channel becomes very noisy. This circuitry can also be used to feed a hit pattern into the pipeline for test purposes.

The pipeline memory stores hits for 132 bunch crossings. It is implemented as a 12 by 12 array of capacitors. Bits are loaded into successive rows of the first column of the array. On receipt of a level one trigger after 128 bunch crossings, the bit from 128 bunch crossings earlier, as well as one older bit and one newer bit, are transferred to the derandomising buffer. This is a 24-bit FIFO, allowing up to 8 events to be stored. It has independent read and write pointers. If the write pointer overtakes the read pointer (due for example to a burst of triggers in quick succession) events are lost, however this condition is flagged in a buffer-overflow bit.

Each set of three bins is sent out via a zero-suppression logic. This logic can be operated in four modes, summarised in Table 3.5. Only a hit pattern appropriate to the mode is recorded. The output consists of the channel numbers of the start of a cluster of hit strips, followed by a list of hit patterns in the strips of the cluster.

The chip can be operated in three modes: master, slave or end. The chips on each side of an SCT-module are configured as master-slave-slave-slave-slave-end. The chips on the front (the connector-side of the hybrid) are called M0-S1-S2-S3-S4-E5. The chips on the back are called M8-S9-S10-S11-S12-E13. Read-out is controlled by token passing and commences with the end chip. On receipt of the token a chip sends its zero suppressed data to its neighbour, which passes it to the next chip. Finally, the master chip receives the data. It also adds its own data, adds a bunch crossing number and a preamble, and sends all the data to the VDC-chip.

The chips have a charge-injection circuitry for calibration. There are four lines, each line connecting to every fourth channel via a 100 fF capacitance. It loads the capacitance with a
Table 3.5: The four modes of the zero-suppression logic. The hit pattern indicates the three bits that are read-out upon receipt of a trigger. The oldest bit is on the left. The one and zero indicate the required state of a bit, an X indicates that the state of that bit is not important.

<table>
<thead>
<tr>
<th>name</th>
<th>hit pattern</th>
<th>usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>hit</td>
<td>1XX, X1X, XX1</td>
<td>detector timing</td>
</tr>
<tr>
<td>level</td>
<td>X1X</td>
<td>normal data taking</td>
</tr>
<tr>
<td>edge</td>
<td>01X</td>
<td>normal data taking</td>
</tr>
<tr>
<td>test</td>
<td>XXX</td>
<td>test mode</td>
</tr>
</tbody>
</table>

voltage-step. A step of 10 mV therefore corresponds with an input charge of 1 fC, equivalent to the charge of 6242 electrons. The exact value of the capacitance is batch-dependent. Each wafer has therefore a few test-structures, on which the capacitance is measured; a hybrid is in general made with chips from the same batch and is supplied with a capacitance correction-factor.
The SCT end-cap detector