Development of Micromegas-like gaseous detectors using a pixel readout chip as collecting anode

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Chapter 5

Fabrication of integrated Micromegas

I present in this chapter the fabrication of integrated Micromegas detectors called InGrids. Measurements of geometric parameters of several InGrids will be summarized, demonstrating that the dimensions of the grids can be controlled to a precision of a few microns. I will discuss the dimension and material limitations and briefly sketch the detector test procedure.

5.1 Introduction

InGrid is a Micromegas grid integrated on a silicon substrate by means of planar microfabrication techniques [181]. It is meant to enhance the performance of Micromegas-based pixel readout detectors. By means of a few post processing steps [176], wafers of pixel readout chips can be equipped with InGrids, paving the way to the mass production of Micromegas pixelated detectors.

The manufacturing techniques provide an accurate control of the grid geometry over areas of a few cm$^2$. The grid can fit any pixel readout chip, with the grid holes precisely aligned with the pixel input pads. Also, the grid-supporting structures (pillars or walls) can be placed in between the pads. Accordingly, the detection efficiency should be uniform across the detector surface and almost all the chip area is active. In addition, the grid dimensions can be optimized for low ion backflow and efficient electron collection and detection.

InGrids are fabricated on 100-mm wafers which act as dummy carriers. Several InGrids of various geometries are made on a single wafer in order to study the impact of the geometry on the operational characteristics. Later on, the process is meant to work on 200-mm and 300-mm wafers.
5.2 Fabrication process

5.2.1 Process flow

The steps of the fabrication process are detailed in the following sections. They consist in wafer cleaning and oxidation, deposition and patterning of the anode material, deposition and exposure of a thick photosensitive film, deposition and patterning of the grid material and finally removal of the photosensitive film through the grid holes. Some of these steps are depicted in Figure 5.1. For more informations on the various microfabrication techniques used throughout the process, the reader is referred to [181, 182].

1. 0.2 µm Si wafer oxidation
2. 0.2 µm anode patterning
3. 50 µm SU-8 coating and exposure
4. 0.8 µm grid patterning
5. SU-8 development

Figure 5.1: Main steps of the InGrid fabrication.
5.2 Fabrication process

5.2.2 Wafer cleaning

During the growth of a silicon oxide layer, it is desirable that the oxidation proceeds uniformly across the wafer surface. For this reason, native oxide and any residual impurities and particles should be removed from the wafer surface prior to the oxidation. The types of impurities likely to exist at the wafer surface include organic compounds and metallic particles. These are generally residues of photoresist or metal films previously deposited on the wafer. At the beginning of the process, we expect a small contamination of these. On the other hand, native oxide forms upon exposure of the wafer to air (e.g. during storage, before the wafer is used). It should be removed if a uniform oxide layer is to be formed during the oxidation.

The cleaning is a sequential procedure to remove organic and metal residues as well as native oxide from the wafer surface. There are different types of cleaning procedures. When cleaning bare silicon wafers, a common wet chemical cleaning procedure consists in dipping the wafer in several acid baths. The first wafer bath is performed in a solution of fuming nitric acid which dissolves the organic compounds. Metallic impurities are removed when the wafer is immersed in a solution of boiling nitric acid. Finally, a solution of hydrofluoric acid is used to remove the native oxide from the wafer surface. After each acid bath, the wafer is rinsed in a solution of de-ionized water to prevent reactions between the different acids.

5.2.3 Wafer oxidation

The InGrids are fabricated on bare silicon wafers which act as dummy carriers. Due to impurities in the bulk, silicon wafers are slightly conducting and it is therefore desirable to electrically isolate the detector anode from the wafer bulk. This is realized by the deposition on the wafer of a layer of insulating material. Silicon oxide with a breakdown voltage of $10^7$ V/cm is well suited for this purpose. We chose to grow a 200 nm thin layer of SiO$_2$ on the wafer surface by dry oxidation. The oxidation proceeds according to the overall reaction:

$$\text{Si(solid)} + \text{O}_2(\text{gas}) \rightarrow \text{SiO}_2$$

Due to a much higher diffusivity of O$_2$ than Si in SiO$_2$, the reaction occurs at the Si-SiO$_2$ interface. At room temperature, however, the oxygen molecules are not sufficiently mobile to diffuse through the oxide. Reaction 5.1 effectively stops after a while and oxide thicknesses of about 25 Å are obtained. The oxidation can be continued by heating up the wafer, which increases the diffusivity of O$_2$ in SiO$_2$. This is realized inside a furnace which once closed, is flushed with oxygen gas. A batch of wafers is placed on a quartz carrier which is then introduced inside the furnace. At a temperature of 800 °C an oxide thickness of 200 nm is obtained after approximately 12 hours.
5.2.4 Anode deposition

The detector anode is a 200 nm thin layer of aluminium formed on the wafer surface by sputtering. The wafer is placed horizontally inside a plasma reactor below a target of the material to be deposited. The reactor is pumped down and flushed with an inert gas (Ar or N$_2$) which is ionized by a discharge. The positive ions of the plasma are accelerated towards the target by a uniform electric field. Upon impact of the ions, some atoms are released from the target and reach the wafer surface.

The sputtering system used provides deposition rates from $10^{-10}^{4}$ nm/min [183]. At the highest deposition rate, a 200 nm thin aluminium layer is formed in a few seconds. It is worth noting that during the deposition, the substrate receives energy from UV photons and electrons produced in the plasma as well as from the target atoms. When sputtering aluminium on substrates that are sensitive to UV light or heat, the substrate chemical properties may change.

5.2.5 Anode patterning

The sputtered Al layer extends all over the wafer surface and is patterned to individual regions by means of photolithography and wet etching techniques. Photolithography is the patterning of a photosensitive film, or photoresist, using light. The patterned film can subsequently be used as mask to treat specific wafer regions underneath (e.g. doping, sputtering, etching). Photolithography proceeds in four main steps some of which are illustrated in Figure 5.2 in the case of an etching process.

- Deposition by spin coating of a thin liquid photoresist which has high absorption coefficient in the UV domain. The photoresist is a mixture of a resin, a photoactive compound and a solvent. The latter controls the mechanical properties of the resin such as its viscosity.

- Evaporation of the solvent by heating up the photoresist (so-called soft-bake). This is realized by placing the wafer on a hot plate.

- Exposure to UV light through a mask, the photoresist chemical properties change in the exposed regions.

- Immersion of the wafer in a specific solution (so-called developer) where either the exposed or unexposed regions of the resist are dissolved, depending on its polarity. In this way a positive or negative image of the mask is printed in the resist.

We spin coat a 1.6 $\mu$m thin layer of positive photoresist over the Al covered wafer. This resist is produced by Fujifilm (OiR 907) and is referred to as 907 in the following. It is patterned to 12 square-shaped regions of $2 \times 2$ cm$^2$ (the wafer design is presented in section 5.3). The patterned film is then used as a mask.
5.2 Fabrication process

Figure 5.2: Main steps of a photolithographic process used to etch specific regions of a film present on the wafer surface.

to etch the Al layer in regions where the photoresist has been developed. The etching is done in a solution of phosphoric acid at a temperature of 60 °C at a rate of about 1.2 μm/min. After rinsing in de-ionized water, the photoresist is removed in a bath of fuming nitric acid. Eventually, one is left with a 100-mm diameter oxidized wafer onto which are printed 12 Al square-shaped regions of $2 \times 2 \text{cm}^2$.

5.2.6 Supporting structures deposition and exposure

A few tens of microns thick layer of SU-8 photoresist is deposited onto the wafer by spin coating. It is then exposed to UV light to define the grid-supporting structures: pillars or walls, outer dikes and grid contact pads. The dikes support the grid on its edges.

SU-8 is a negative tone, near-UV photoresist whose absorption spectrum peaks at 365 nm. Due to its high viscosity, structures with thicknesses up to 2000 μm can be patterned with large aspect ratios. These features make SU-8 a very attractive material for fabrication of MEMS and micro-sensors [184, 185]. Studies of the use of SU-8 for building radiation detectors are also reported in [186, 187].
SU-8 consists of a polymeric epoxy resin dissolved in an organic solvent to which is added a photosensitive salt. Upon exposure to UV light, the salt generates an acid which acts as a catalyst in the reaction between epoxy groups. On average, a single molecule has eight epoxy groups (hence the name SU-8) and this reaction results in a dense network of chemical bounds (so-called cross linking reaction). As this reaction is very slow at room temperature, the SU-8 film is heated up to accelerate the cross linking reaction (so-called post-exposure bake). After cross linking, the exposed regions are insoluble in the SU-8 developer.

The film is deposited on the wafer by spin coating and its thickness is chosen according to the desired InGrid amplification gap thickness, generally between 30 and 100 μm. Measurements of thickness variations across the wafer surface are reported in section 1.4.2. The film is soft-baked approximately 1 hour at 120 °C to evaporate the solvent and slowly cooled down to room temperature. During the soft-bake, important internal thermal stress is generated in the film. To release that stress, the wafer is left 24 hours at room temperature. Afterwards, the SU-8 film is exposed to UV light during a few tens of seconds, the precise exposure time being adjusted to the SU-8 thickness and the amount of photoacid generator present in the film. A post-exposure bake of 1 hour at 95 °C is performed to accelerate the cross linking reaction in the exposed SU-8 regions. Again, the resist is slowly cooled down to room temperature and 24 hours are awaited before resuming the process.

The SU-8 layer is not developed yet. Instead it is used as a sacrificial layer for the deposition of the grid metal layer. Pictures of SU-8 structures where the photoresist has been developed before the formation of the grid are shown in Figure 5.3.

![Figure 5.3: Pictures of pillars (a) and walls (b) supporting structures.](image)
5.2 Fabrication process

5.2.7 Metal layer deposition

The grid is formed by sputtering on the SU-8 surface a thin layer of aluminium which is then shaped into a grid by wet etching. Aluminium exhibits low residual stress, it can be easily etched and shows good adhesion with SU-8 [188]. The sputtering of the aluminium layer on the SU-8 surface is realized in the reactor used for the anode deposition.

The grid thickness should be such that the grid is sufficiently rigid and does not bend when applying high voltage across the amplification gap. Standard Micromegas grids have thicknesses of at least 5 \( \mu \text{m} \) and one may want to start with such values. Unfortunately, the grid thickness can not be increased at will because the chemical properties of SU-8 are expected to change during the metal deposition. In particular, UV light produced in the glowing plasma may initiate the production of acid at the surface of the unexposed SU-8 regions. Therefore, local increases of temperature across the SU-8 film surface may initiate the cross linking reaction, preventing a complete development of the SU-8 unexposed regions. This increase can be due to the photons, electrons and target atoms striking the substrate and also by the heat-of-condensation of the depositing film [189].

For this reason, a 1 \( \mu \text{m} \) thin layer of 907 positive photoresist is deposited over the SU-8 and both resists are exposed simultaneously. The positive resist is developed prior to the metal sputtering such that the unexposed regions of SU-8 are, to some extent, protected against the UV light. The resist is later removed in the SU-8 developer. Also, the metal is sputtered in several short steps. Between each step, the wafer is brought out of the reactor to a loadlock where a flow of N\textsubscript{2} gas cools the substrate surface to room temperature. Repeating those steps a reasonable number of times, an aluminium thickness of about 1 \( \mu \text{m} \) is obtained.

5.2.8 Grid hole etching

The patterning of the aluminium layer to the desired grid geometry is realized by photolithography. The soft-bake, however, can not be performed. Despite the additional photoresist layer, some acid could have been produced during the sputtering and the SU-8 film should not be heated anymore. Instead, the wafer is left 3 hours at room temperature before exposure of the photoresist. The etching of the grid is performed in a solution of phosphoric acid at room temperature resulting in an etch time of roughly 40 minutes. The etch rate is slightly higher for holes with large hole diameters than for holes with smaller ones. Because the etching is stopped when the small holes are opened, the diameters of large holes generally exceed their design values. Measurements of hole diameter variations are reported in section 5.4.2.
5.2.9 Wafer dicing

It will be of interest to have at the same time in the test chamber InGrid detectors from different wafers. If, for instance, InGrids of different amplification gap thicknesses should be tested in a row, several wafers would have to fit in the chamber. The dimensions of the chamber, for practical reasons, cannot match this requirement. Instead, the 12 InGrids are diced to individual wafer pieces of $2 \times 2$ cm$^2$, each InGrid being equipped with anode and grid contact pads. The dicing is performed prior to the SU-8 development, otherwise the InGrids would be easily damaged during the dicing.

5.2.10 SU-8 development

After dicing, one proceeds to the development, through the grid holes, of the unexposed regions of SU-8 and of the additional 907 positive resist. During the development, the adhesion of the grid onto the supporting structures is sometimes not sufficient and the grid peels off. Therefore the development should be stopped as soon as no SU-8 is seen flowing through the grid holes. Although SU-8 has its specific developer, acetone is preferred as it was observed that the development proceeds faster in this solution. According to the SU-8 processing rules, isopropanol is used to rinse the InGrid after the development.

Hence, individual InGrids are dipped in acetone until no SU-8 is seen flowing through the grid holes and rinsed with isopropanol. Sometimes, unexposed regions of SU-8 are not properly dissolved after rinsing and additional baths in both solutions are performed. The duration and the number of baths required for a complete development vary from wafer to wafer and were observed to depend strongly on the grid metal sputtering recipe. In particular, when the sputtering steps are too long or when the wafers are not vented sufficiently between these steps, several baths are performed.

This is interpreted as follows: during the aluminium deposition, the chemical properties of the SU-8 unexposed regions change from the SU-8/907 interface until a certain depth in the SU-8. The thickness and composition of this intermediate layer probably correlate to the temperature of the SU-8 surface and the number of absorbed photons, during the sputtering. If these are kept low enough, the intermediate layer is thin enough for acetone to break through and SU-8 is readily developed. On the other hand, if these are too high, that layer does not dissolve in acetone and no development takes place. A picture of a grid after SU-8 development is shown in Figure 5.4 (a).

5.2.11 Plasma cleaning

After the SU-8 development, residues of the interface layer are etched in a plasma reactor. A batch of InGrids is placed in a quartz carrier which is brought inside the reactor. The reactor is pumped down to pressure of a few millibars and filled
5.3 InGrid wafer designs

Photolithography techniques permit an accurate control of the detector amplification gap thickness, hole pitch and diameter. It is interesting to study how the mechanical and operational characteristics of InGrid detectors depend on these geometrical parameters. Hence, four wafer designs were successively realized, all consisting in a large variety of geometries with various hole pitches and diameters.

One of the first designs contained 18 $177 \text{ mm}^2$ round-shaped InGrids with various supporting structure dimensions. It was mainly intended to determine which pillar configurations would provide enough support. The latest design consists of 12 $314 \text{ mm}^2$ InGrids of 4 different hole pitches (20, 32, 45 and 58 $\mu$m) with holes placed according to a square pattern. The hole diameters of InGrids of same pitch are roughly equal to $1/3$, $1/2$ and $2/3$ of the pitch. Also, the layout of the 12 InGrids is such that the wafer is easily diced to individual prototypes. A pillar diameter of 30 $\mu$m is adopted. For InGrids with hole pitches of 45 and 58 $\mu$m, the pillars are placed in between the holes. The pillars are placed according to a square pattern and their pitch is adjusted to the hole pitch, between 90–128 $\mu$m.

Figure 5.4: View of a grid after the development of the SU-8 layer (a). The residues of the interface layer around the holes are etched in a plasma reactor (b). The misalignment between the pillars and the grid was due to a loss of contact during the SU-8 development.
5.4 Geometry uniformity

It was of interest to quantify how precisely the detector geometry can be controlled. In this section, I report on measurements of amplification gap thicknesses and grid hole diameters performed on InGrids from five wafers.

5.4.1 Amplification gap thicknesses

Gap thicknesses were determined by measuring step sizes between the wafer surface and the SU-8 dikes. Step sizes were measured by means of a Dektak [190]: a thin needle tip free to move vertically is dragged horizontally over the wafer surface and its vertical displacements reflect the topography underneath with an accuracy of a few tens of nanometers.

InGrids from the 5 wafers were placed below the Dektak tip, for each one the dike heights were measured on 4 different locations. All gap thicknesses exceeded by 10–20 % the expectations from the SU-8 deposition system, however, variations at the wafer level were below 5 % r.m.s.. At the grid level, gap variations below 1 % r.m.s. were measured.

The SU-8 layer is deposited by spin coating and its final thickness depends on the spin coater rotation speed and the photoresist viscosity. The latter relates to the fraction of solvent mixed with the photosensitive compound. When SU-8 is stored for several days in its container, some solvent evaporates, resulting in larger viscosities and therefore larger thicknesses. This explains the 10–20 % discrepancies between measured and expected thicknesses.

5.4.2 Hole diameters

Hole diameters were measured by means of a microscope with a precision of 0.5 \( \mu m \). First, hole diameters of 5 InGrids from a same wafer were measured on 5 different locations across the grids. The diameter standard deviations were all below 1 \( \mu m \). Secondly, differences between measured and design-on-mask hole diameters were determined for most InGrids of 3 wafers. In this case a single measurement per InGrid was realized. The measurements showed that the grid hole diameters exceed the design-on-mask values by 1 to 8 \( \mu m \).

5.5 Processing considerations

5.5.1 Largest amplification gap thickness

The maximum thickness of the amplification gap depends on the aspect ratio of the SU-8 supporting structures. In the case of pillar-like structures, aspect ratios up to 4 are used. With a pillar diameter of 30 \( \mu m \), the pillar heights should not exceed 120 \( \mu m \). This is not problematic as there are no strong motivations to fabricate InGrids with gaps larger than 100 \( \mu m \).
5.5.2 Distance between pillars

The distance between pillars is important for the adhesion of the grid on the pillars. Also, it determines the flatness of the grid: if the distance between pillars is too large the grid may bend towards the anode. The effect may be accentuated when negative voltage is applied to the grid (while the anode is connected to ground) as the electric force pulls the grid towards the anode. Accordingly, the amplification gap thickness may be higher close to the pillars than in between the pillars. For certain gap thicknesses, this should result in gain variations from hole to hole.

Although pillar pitches as large as 240 \( \mu \text{m} \) for a triangular pattern of 40 \( \mu \text{m} \) diameter pillars showed good operational characteristics [177], they could not be fabricated in a reliable way. In some cases, due to a poor adhesion, the grids peeled off locally or completely during the SU-8 development. We therefore adopted pillar pitches ranging from 90 to 128 \( \mu \text{m} \) (for a square pattern of 30 \( \mu \text{m} \) diameter pillars). These smaller pitches, together with some process improvements, showed increased fabrication yield.

5.5.3 Smallest hole diameter

The InGrid with the smallest hole diameter that could be fabricated and tested has a hole diameter of 10 \( \mu \text{m} \). The etching of such small holes takes more time than that of larger holes. This is because the by-products of the reaction between the acid and the metal are less quickly removed from the aluminium surface and prevent fresh acid molecules to reach this surface. The etch rate can be increased by a constant stirring of the acid solution and one could in principle go to smaller diameters.

In typical working conditions of an InGrid detector, the mean free path of an electron in the gas is about a few microns. When approaching the grid, the probability that the electron hits the grid and is not detected increases when the hole diameter is reduced (see section 6.3.2 for experimental measurements). From the functional point of view, it is thus not worth going to hole diameters smaller than 10 \( \mu \text{m} \).

5.5.4 Largest hole diameter

The largest hole diameter is limited by the hole pitch. On the functional side, holes with large diameters facilitate the passage of the electrons through the grid but degrade the electric field uniformity in the amplification region. If the field is not uniform at the entrance of the amplification region, the gain may depend on where the electrons enter the hole. This introduces additional gain fluctuations and therefore the hole diameter should not be too large, especially for small amplification gap thicknesses (see section 6.7.3 for simulation results).
5.5.5 Grid thickness and material

The grids are made of 1 $\mu$m of metal and are very fragile, the InGrid detectors are hence easily damaged during manipulation or testing. For instance, the resistance to gas discharges is poor as the metal locally vaporizes. That could be improved with the deposition of thicker layers and the use of conductive materials with a higher heat capacity.

So far, trials to sputter aluminium layers thicker than 1 $\mu$m resulted in wrinkles on the metal film surface and in an incomplete SU-8 development. Similar observations were made when trying to deposit materials other than Al like TiW, Cu, aSi or Au. Other deposition techniques like evaporation or electroplating are being investigated but did not produce testable prototypes yet [191].

Another important aspect related to the grid thickness is the field shape in the vicinity of the hole edges. Due to the sharpness of the grid close to these edges, we expect there an electric field stronger than in the amplification region. Electrons entering the amplification region close to a hole edge may experience more ionizing collisions than an electron entering in the center. In those cases, the gain and the discharge probability may increase significantly there.

5.6 Detector testing

The $2 \times 2$ cm$^2$ individual InGrids are mounted on thin PCB boards for easier manipulation (Figure 5.5). The boards are $2 \times 2.5$ cm$^2$ and are equipped with two contacting pins to which are soldered the anode and grid HV wires. Two thin wires are used to connect the InGrid pads and the board pins and are silver-glued to these electrodes on both ends. The test chamber can house up to 6 InGrid carrying boards.

5.7 Conclusion

The techniques of photolithography, wet etching and sputtering permit a large variety of detector geometries to be fabricated with high precision. With SU-8 as a pillar material, amplification gap thicknesses from 30 to 100 $\mu$m can be realized with variations less than 1 % at the grid level. Hole diameters down to 10 $\mu$m could be controlled with a precision of 1 $\mu$m. This accurate control on the detector dimensions promises a very good gain uniformity across the grids.

The choice of grid material is driven by yield reasons. The sputtering of a 1 $\mu$m thin layer of Al on SU-8 does not prevent the subsequent development of this photoresist. This is unfortunately not the case when depositing thicker layers or materials of higher heat capacity which are desirable to improve the resistance of the grid against gas discharges. As a result, only InGrids made of Al were tested sofar. Measurements of their amplification properties are reported in the next chapter.
Figure 5.5: A 2 cm diameter InGrid mounted on a board for test.