Bose-Einstein condensates in radio-frequency-dressed potentials on an atom chip

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3 Atom chip fabrication and characterization

3.1 Introduction

This chapter serves as a record of the fabrication procedures used to create an atom chip incorporating extremely long, narrow and straight wires for producing magnetic potentials for trapping atoms, and as a guide for future researchers aiming to produce their own atom chips. It is organized as follows. Section 3.2 gives general information on the atom chip and its fabrication and discusses the design considerations. Sec. 3.3 treats the actual microfabrication recipe in detail. The design of the wire pattern is shown in Fig. 3.3 and described in Sec. 3.4. The properties of the resulting chip wires are the topic of the following section 3.5. Finally, Sec. 3.6 contains the conclusions with regard to the atom chip fabrication and characterization.

3.2 Design considerations

Before describing the fabrication protocol in detail, we give an overview of the most important features of the chip, the fabrication process and the considerations that led us to choose this process and feature set. Two factors played an important role.

First of all, we aim to produce well-defined, and possibly even tailored trapping potentials, such as those needed to study quantum gases in the 1D regime [73]. From earlier studies [114] it is clear that the techniques chosen for the fabrication to a large extent determine the quality of the current-carrying wires and the smoothness of the resulting trapping potentials. The desired fine structured trapping potentials also require that the atoms are trapped in close proximity to the wires and the chip should allow for this. Second, the goal was to keep the process as simple as possible in order to save on the time spent on mastering the fabrication process and on the fabrication in general allowing many chip designs to be implemented in a short time. So instead of making a complex atom chip, we decided to make a simple chip that would enable us to do the experiment(s) we had in mind. The vicinity of and our direct access to the cleanroom of the Amsterdam nanoCenter made this a natural choice for the fabrication to take place. Thus, the process described below was developed in close collaboration with its main engineer, Chris Rétif, and makes optimal use of the facilities available there.

Driven by our desire to create 1D magnetic potentials we decided to use an atom

chip employing current-carrying wires instead of magnetic thin films, because such a wire chip is very well suited for making elongated potentials. To reduce complexity as much as possible we decided to have only one conducting layer on our chip. This imposes some restrictions on the wire pattern as it is impossible to let the wires cross each other, but it greatly simplifies the fabrication process.

To allow for tight traps that are also sufficiently deep, it is important to maximize the current in the chip wires. And since ohmic heating of the wires is usually the limitation we wanted to make our chip of materials that are good heat conductors. We chose gold for the conducting layer material and silicon for the substrate. Apart from their good thermal conductivity these materials have the advantage that they are commonly used in microfabrication and ample experience processing them is available at most microfabrication centers.

The maximum current in the chip wires depends strongly on the thickness of the gold layer. To produce a magnetic trap deep enough for reaching BEC in a Z wire trap (see Ch. 2) we require at least 2 A of current. In a 100 μm wide, 2 μm thick wire that would amount to a current density of 10^6 A/cm^2 which is lower than values reported in literature [115], though the wires in this reference were made of copper, not gold. Also such a wire with a length of $\sim$5 mm has an estimated resistance of 0.5 Ω. The corresponding dissipation 2 W is low enough to allow it to be cooled by conduction through the silicon substrate.

To fabricate the gold layer, which is rather thick to microfabrication standards, we chose to use two layers of resist. The top layer is a photo-sensitive resist that is patterned using optical lithography. The bottom layer is a lift-off resist, which acts as a spacer that lifts up the top layer and prevents it from being buried under the gold (see Fig. 3.1). We chose to deposit the gold on our chip through the process of evaporation because (i) this process is known to produce very smooth wires and (ii) because this technique was readily available to us at the Amsterdam nanoCenter.

We selected a substrate thickness of 300 μm, for which 3" wafers are readily available. This is sufficiently thin for the magnetic field of the miniwires to be effective (see Ch. 2 and also [88]), while sufficiently thick that inadvertent breaking of substrates during microfabrication and gluing is rare. For electrical insulation between the chip wires we rely on (i) the resistivity of the silicon which we took as large as possible and (ii) the native silicon oxide layer, a thin layer of oxide that is present on all silicon surfaces exposed to air. Not adding an extra oxide layer on the substrate surface helps to keep the fabrication process simple while also maximizing the thermal contact between the wires and the substrate.

Finally, we decided to use the mirror-MOT technique [116] for the initial optical cooling, where two of the beams reflect off the chip surface. To enable the mirror-MOT technique we have to make the chip at least as large as the MOT laser beams (15 mm, $1/e^2$ beam diameter). On the other hand the chip size is limited by the CF40 flange through which the chip enters the vacuum system. We make the chip reflecting at 780 nm by covering the area in between the wires also with gold which has an excellent reflectivity at this wavelength [117]. The light scattering off the narrow trenches that define the chip wires we take for granted.

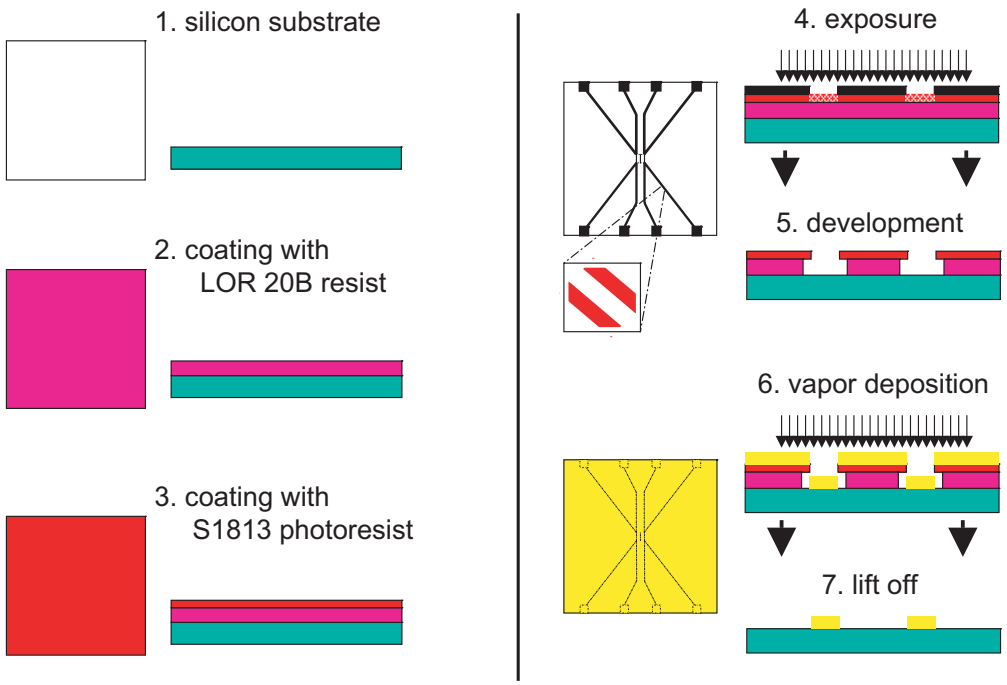

Figure 3.1: Schematic representation of the atom chip fabrication process. The substrate is cut to size (1) and two layers of resist are applied (2,3). After exposure to NUV light (4) and development (5) the edges of the resist have an undercut of $\sim$1 μm. Gold is vapor deposited on the entire chip (6), after which the superfluous gold is removed through lift off (7).

3.3 Fabrication protocol

The fabrication process is summarized in Fig. 3.1. The substrate is coated with two layers of resist and is patterned using optical lithography. In the following development the lower resist layer dissolves faster than the top layer, automatically generating the typical shape, called undercut, in which the top extends over the bottom layer. A layer of gold is deposited through vapor deposition. By virtue of the overhang the edges of the deposited gold are well-defined, while the open structure allows exposure to a solvent. The solvent dissolves the resist effectively removing the gold lying on top of it. This technique is known as lift-off. What remains is a patterned gold layer on the silicon substrate. The fabrication process is described in more detail in the following paragraphs, and Fig. 3.2 shows some microscopy images taken at various stages of the process.

Preparation of the substrate

Substrates are cut from 3" silicon wafers with a (1-1-1) crystal orientation, a thickness of 300 μm and a resistivity of at least 4000 Ωcm. We selected this silicon because of the thickness and the large resistivity. Atom chip substrates were produced from the wafers by laser cutting at the Energy research Centre of the Netherlands (ECN) in Petten. The dimensions of the resulting substrate are $24.63 \times 16.00\,\mathrm{mm}^2$. We

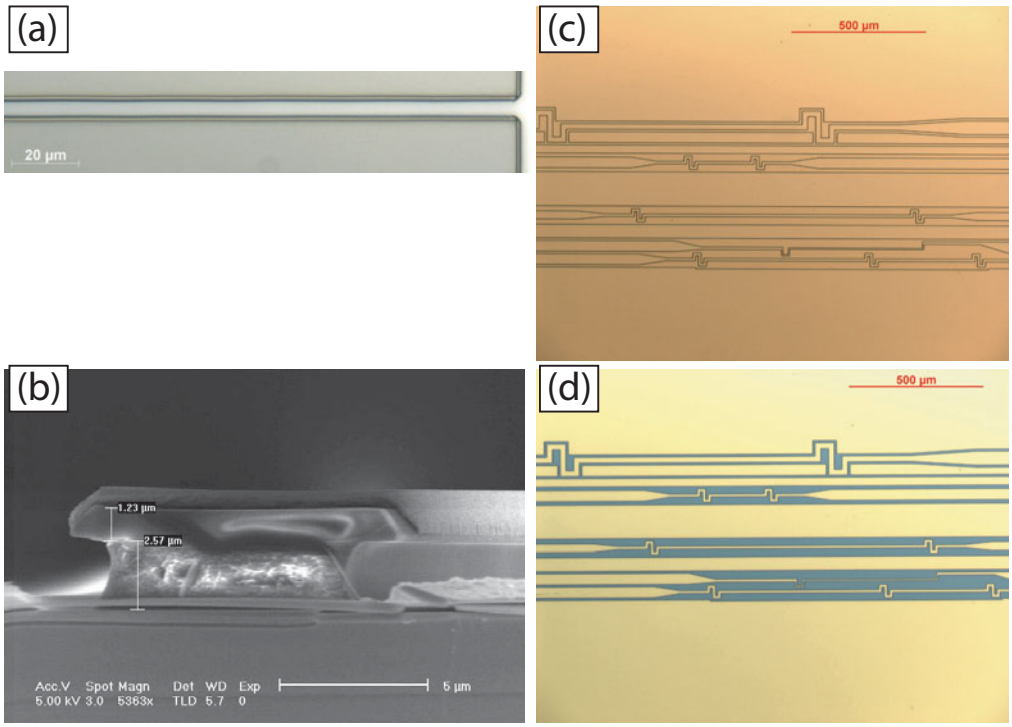

Figure 3.2: Microscope images of atom chips at various stages of the fabrication process. (a) Optical microscope image of the resist structure for a single 5 μm wide wire. The undercut shows up in the image as a double line edge. (b) SEM image of the cross section of a chip after gold evaporation. Both images show the resist structure with undercut and a layer of gold on top. Optical microscopy images of the actual chip used for the experiments described in this thesis after gold evaporation (c) and after lift off (d).

clean the substrate prior to microfabrication in an ultrasonic bath, a hot ammonia solution and a hot hydrogen-peroxide solution to remove possible Si debris and any hydro-carbons attached to the surface.

Resist

We dry the substrate prior to applying the resist, because water adhering to the silicon surface has a detrimental effect on the resist. The substrate is dried on a hot plate at 150°C for 5 minutes. After the substrate has cooled down we apply the first layer of resist by spin coating. The viscous lift-off resist LOR 20B forms a 2.5-μm-thick layer after spinning for 1 minute at 3000 rpm. The exact thickness of the layer varies depending on air humidity (this is not controlled independently at the Amsterdam nanoCenter), but is at least 2.0 μm. The substrate is baked again 5 minutes at 150°C. The second layer consists of Microposit S1813, a positive photoresist. It is applied by spin coating for 1 minute at 5000 rpm and forms a layer of 1.2 μm thick. After baking for 30 minutes at 90°C the resist is photosensitive.

Optical lithography

The resist is exposed for 7.4 s to the 10-mW/cm^2, 365-nm near-ultra-violet (NUV) light of a Karl Suss MJB3 mask aligner. The mask is a 4" Cr mask that was made to specification by Deltamask (Enschede, The Netherlands). This company fabricated it with a 442-nm HeCd laser with a resolution of $\sim$1 μm, based on a design drawing in AutoCAD. In our case the practical resolution is not limited by the lithography mask, but by scattering and divergence of the light inside the thick bilayer resist to about the total thickness of the resist layer ($\sim$3 μm). The mask tends to contaminate (and even damage) with use, because it is pressed on the substrate during exposure. To extend the lifetime, the mask contains four identical copies of the atom chip wire pattern. As one copy degrades we simply switch to the next to continue fabrication.

The exposure is followed immediately by development. We submerge the substrate for 1 minute in Microposit MF319 developer after which it is rinsed in water to stop development. The undercut, the typical structure with the top resist layer extending $\sim$1 μm over the edge of the lower layer, comes about automatically in development as the lower layer dissolves faster than the top layer. Prior to gold evaporation we expose the chip to a low-energy oxygen plasma for 5 minutes to remove possible resist residue from the exposed silicon.

Gold deposition

The gold layer is deposited at $\leq 10^{-5}$ mbar in a PVD (Physical Vapor Deposition) system. First we deposit a 2.5 nm layer of titanium at a rate of 0.1 nm/s as adhesion layer between the silicon and the gold. We have also tried chromium as adhesion layer. Mechanically both materials appear to do equally well, but titanium was chosen because it is nonmagnetic, avoiding possible complications due to magnetization of the Cr layer.

Next we evaporate the gold at a rate of 1 nm/s. The crucible in the PVD system can only hold 3 g of gold at a time, enough for a 1.25-μm-thick layer. After a refill we continue the evaporation until the final thickness is reached (typically 2.0 μm). The thickness of the gold layer has to be less than the thickness of the LOR 20B resist layer, otherwise lift off does not work.

Lift off

We leave the chip in a beaker containing Microposit Remover 1165 with a temperature of 68°C for $\sim$1 hour to lift off the superfluous gold. It was found to be helpful to create a bit of flow in the beaker with a syringe. We do not use ultrasonic agitation as that can damage the remaining gold structures. Normally we move the chip to a beaker containing clean Remover fluid once or twice, to reduce changes of gold shreds re-depositing on the substrate.

After lift off we rinse the chip several times in acetone and iso-propanol to make sure no remover fluid stays behind. Finally we use the oxygen plasma again to remove any remainders of resist or solvent.

Chip mount

Microfabrication is now complete. After initial characterization with optical microscopy, Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) (described in section 3.5), the chip is glued onto a custom-built chip mount with Epo-tek 377 epoxy. The chip wires are connected to the sub-D-type pins on the chip mount via wire bonding. Each contact pad on the chip is connected with 10 bonds of 25-μm-diameter, $\sim$1 mm-long aluminium wires, except the 125 μm-broad Z-wire that has 14 bonds to support the high current (up to 3 A) that will be sent through this wire. The chip mount is described in more detail in section 4.2.4. See also Sec. 3.3 and 3.4 of [88].

3.4 Wire pattern design

Figure 3.3 shows the wire pattern on the chip as used in the experiments of Ch. 5 and Ch. 6. The properties of the wires are listed in table 3.1. The design is centered around a 125-μm-wide Z wire. The length of the central section is 3 mm and is necessary to make the initial magnetic trap large enough to hold sufficient atoms. The width is necessary to carry 2.25 A of current during compression while keeping the dissipation below 4 W. As explained in Ch. 2 the overall Z shape is necessary to provide three dimensional confinement, required to capture and evaporatively cool large numbers of atoms.

As a consequence of the choice for a single conducting layer and a Z shaped central wire, all other wires also have an overall Z shape. Wires 3 and 7 are Z wires with widths of 50 and 30 μm respectively. Their smaller width allows their use as tighter Z traps, because of the larger magnetic field gradients possible. In the experiments described in this thesis, however, they are used to generate the radio-frequency dressing field. Their almost symmetric positioning at a distance of $\sim$100 μm around the 125-μm wire, results in the two field components being nearly orthogonal, so that it is easy to change the direction of the linearly polarized rf field.

The remaining wires have wiggles that define 1D box potentials. The length of the wire section in between two wiggles determines the length of the box. Because of the overall Z shape of these wires the resulting box potential also has a harmonic component. The harmonic component scales with the height of the atoms above the chip surface and as the boxes were designed to trap atoms as close as 20 μm from the surface, the harmonic component is small. Experiments using box potentials will be the topic of future work. Wire 6 was used to generate the oscillating magnetic field for rf evaporation and rf spectroscopy.

In the center of the chip the exact shape and quality of the wires are crucial because of the close proximity of the trapped atoms. Outside the central section the exact current path is less critical. We let the wires fan out as much as possible to reduce wire resistance and thus heat dissipation. Along the long edges of the chip 2.1-mm-wide contact pads provide ample space to connect each wire with wire bonds to a contact pin on the chip mount. The 125-μm-broad Z wire has a wider 4.4 mm pad. The short edge of the chip does not have contact pads. The connecting

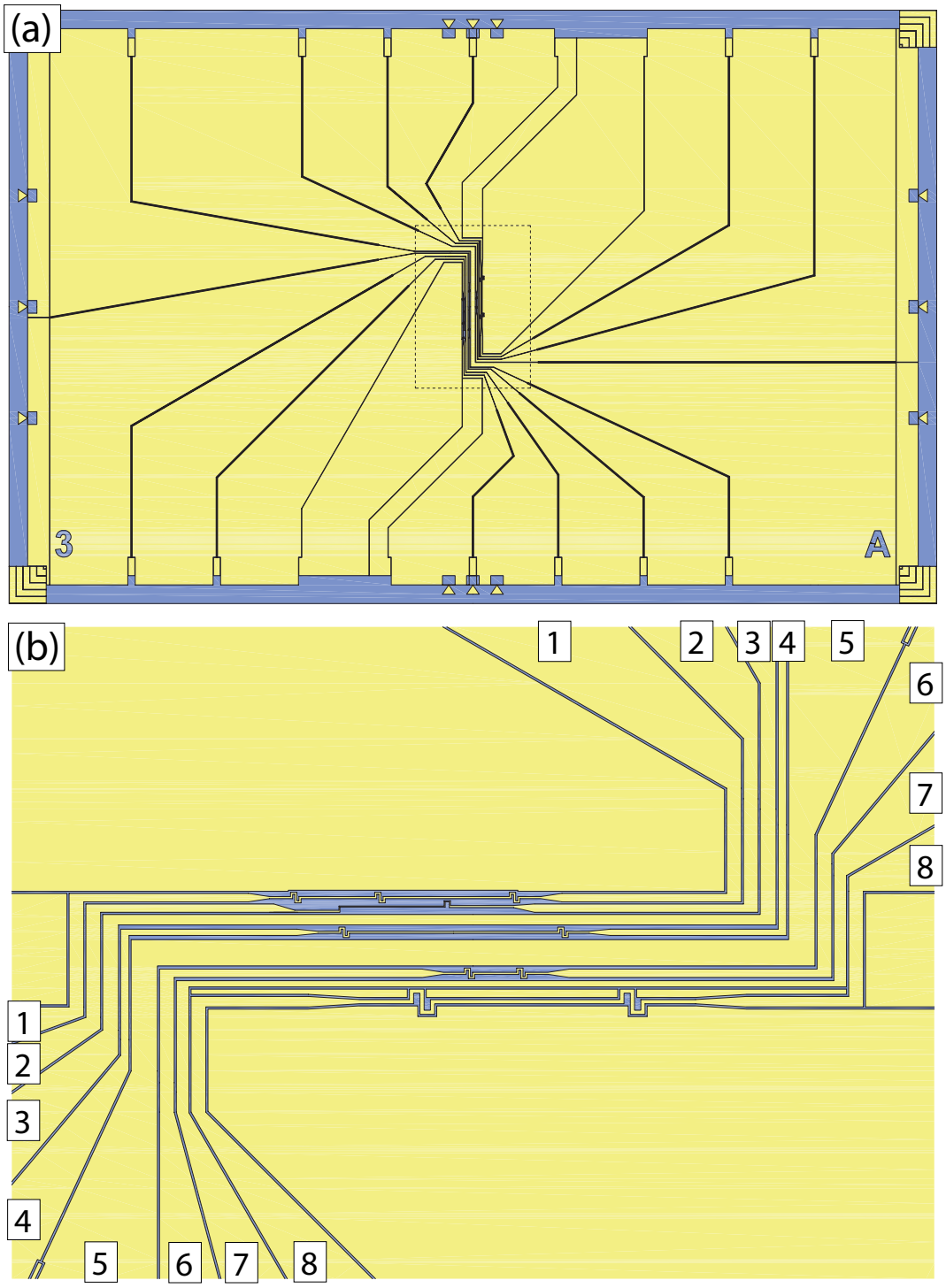

Figure 3.3: Atom chip wire pattern. The area in blue corresponds to the uncovered silicon substrate, while yellow represents the conducting gold layer. (a) Overview of the complete chip. The dashed rectangle measures 3.1×4.3 mm^2 and is shown (rotated 90 degrees clock-wise) in (b). The wire numbers correspond to the numbers in table 3.1.

wire	minimum width (μm)	calculated resistance (Ω)	measured resistance (Ω)	function
1	10	2.93	3.15	double box structure
2	5	3.32	3.70	wiggle test wire
3	50	1.33	1.47	Z wire, radio-frequency field
4	10	3.18	3.89	1.00 mm long box
5	125	0.65	0.72	Z wire, initial trapping and cooling
6	10	2.30	2.42	0.20 mm long box, rf evaporation
7	30	1.83	2.06	Z wire, radio-frequency field
8	20	2.19	2.30	0.90 mm long box

Table 3.1: Properties of the wires on the chip. The experiments described in this thesis utilize wire 5 for the static magnetic trap, wires 3 and 7 for the rf-dressing field and wire 6 for the forced rf evaporation field and the rf spectroscopy field. The other wires are not used.

wire bonds would obstruct the light beam propagating just above the surface of the chip for absorption imaging. The total number of wires on the chip is limited by the number of connecting pins on the chip mount (currently 32 of which 12 are reserved for miniwires).

In the center of the chip neighboring wires are separated by 10-μm-wide gaps in the gold layer. Outside the center, where more space is available, the wires are separated by a 20-μm-wide gold strip in between a pair of 10 μm gaps. This double-groove structure reduces the risk of shorts due to fabrication flaws, while maximizing NIR reflectivity. The sections of the gold layer that are not part of a wire, like the 20 μm strips in between wires, are left electrically floating.

Finally, the edge of the chip contains several markers. Small triangles align with the designed position of the miniwires underneath the chip. The square structures in the corners are used to align the lithography mask to the substrate during microfabrication.

3.5 Wire characterization

3.5.1 Thickness and surface properties

Figure 3.4 shows the resulting wire structures after finishing microfabrication. The typical gold grain size in the deposited layer is 50 nm as can be seen in the SEM image in Fig. 3.4(a). The AFM data in Fig. 3.4(b) gives a similar picture. In a larger SEM image [Fig. 3.4(d)] we see that the top surface and the sides of the wire are smooth down to the grain size of the gold. The finite resolution of the fabrication process is expressed in the smoothing of the corner. The fact that the gold layer was evaporated in two stages can be seen as a change in structure in the side of the wire, though it does not appear to increase the wire surface roughness. Roughness of the wire edge on length scales comparable to the cold atoms–wire separation ($\sim$100 μm)

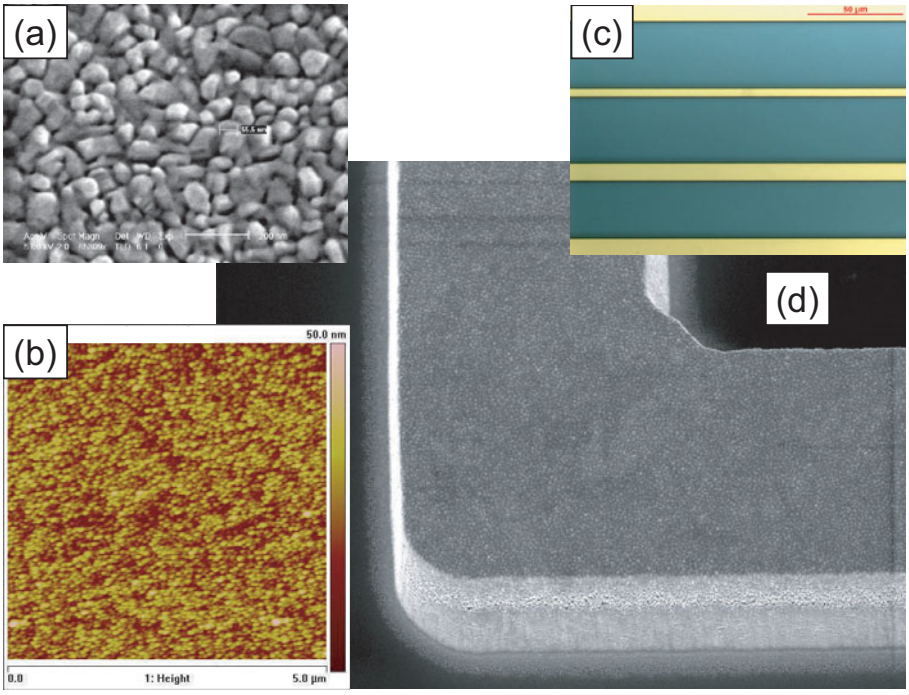

Figure 3.4: Atom chip wires characterized in 3 different ways. (a) SEM image revealing the grainy structure of the gold that makes up the chip wires. The typical grain size is 50 nm. The scale bar at the bottom indicates 200 nm. (b) image of the gold grains obtained with an Atomic Force Microscope (AFM). Image size is 5×5 μm^2 and the color scale extends over 50 nm. (c) Optical microscopy image of several wires. In this image there is no structure visible in the wires and the wire edges appear straight and without any roughness. The scale bar in the top right corner is 50 μm. (d) SEM image of a corner in a 5 μm wide wire, viewed under an angle. The gold layer can be seen to be deposited in two steps. The edges of the wire appear to be straight down to the gold grain size. The dark stripes on the wire near the top and righthand edge of the image are due to electron beam irradiation in the SEM and not due to the fabrication process.

is generally difficult to detect in SEM data because of deformations of the electron beam scan field. In optical microscopy this problem is less pronounced, but the resolution of optical microscopy is insufficient to detect small edge fluctuations that may affect the magnetic potentials experienced by atoms. In the optical microscopy image of Fig. 3.4(c) the wires appear perfectly straight within the optical resolution of $\sim$1 μm.

Using a surface profiler (KLA Tencor Alphastep 500) we have also looked at the flatness of the top surface of a chip wire over a distance of several 100 μm [Fig. 3.5(a)]. The observed high-frequency variation is less than the gold grain size which is intuitively clear as one realizes that the tip of the profiler is significantly larger, effectively smoothing the signal. On longer length scales the variation in wire thickness is comparable to the flatness of a clean silicon substrate which is plotted in Fig. 3.5(b) for comparison. From these and similar measurements we conclude that we can fabricate the intended wire pattern with high quality which should produce

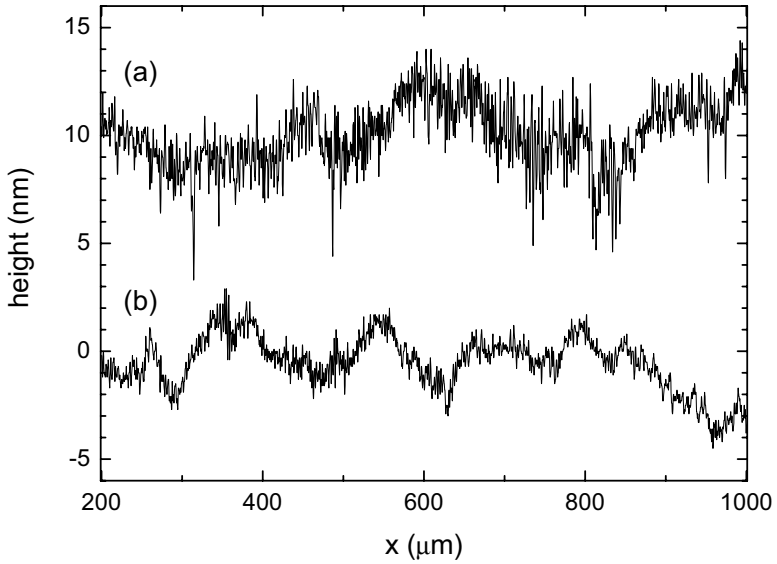

Figure 3.5: Surface profiles measurements of a cleaned bare silicon substrate (b) and a ∼1.2 μm gold layer (a). The offset of curve (a) is chosen such that the average lies 10 nm above (b). The scan speed was 10 μm/s and the horizontal resolution 0.20 μm. Each curve was obtained in a single run.

very smooth potentials.

Using the same surface profiler we have also determined the thickness of the gold layer after completing microfabrication. To exclude damage to the wire structures we measure the thickness of the gold layer in the four corners of the chip. The average of these measurements is the assumed thickness of the gold wires in the center of the chip, which is 1.84 μm for the actual chip used in the experiments of Chs. 5 and 6. Often we find a small gradient (of about 4 nm/mm) in the thickness of the gold layer over the chip which we attribute to the chip not having been directly over the gold crucible during evaporation of the conducting layer.

3.5.2 Chip wire resistance

Prior to fabrication we estimated the chip wire resistances to check if the wires would be able to carry the desired current. Because of the varying wire width, the resistance can not be calculated naively with

$$R = \frac{\rho_0 L}{hw}, \tag{3.1}$$

where ρ_0 is the resistivity of gold at room temperature and L, h and w the wire length, thickness and width respectively. On the other hand a full numerical calculation is needlessly complex. An acceptable solution is to divide the wire in pieces, isosceles trapezoids, with constant width or a width linearly varying along the length, each with a resistance R_i. The R_i of pieces with constant width is calculated with

Inter chip wire resistance (kΩ)																
	Immediately after fabrication								After 3 months of use							
1																
2	560								15							
3	496	437							31	7.2						
4	443	384	338						12	9.0	1.1					
5	394	270	226	127					13	8.2	1.6	0.73				
6	500	437	399	196	244				19	16	8.5	6.5	4.9			
7	610	536	500	437	336	360			50	43	16	13	11	7.7		
8	752	690	651	590	477	536	572		76	67	53	48	46	45	16	
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8

Table 3.2: Electrical resistance between chip wires. The wire numbers along the left and bottom edge of the table correspond to the numbers in Fig. 3.3.

Eq. (3.1) while the R_i of the other pieces is found by integrating the local resistivity along the wire:

$$R = \int \frac{\rho_0 dl}{hw(l)} = \frac{\rho_0 L}{h} \frac{\ln(w_1/w_2)}{w_1 - w_2}, \tag{3.2}$$

where w_1 and w_2 ($w_1 \neq w_2$) are the widths at both ends of the wire piece. The total estimated wire resistance R is obviously the sum of all R_i.

We measured the real resistance of the chip wires after the chip was glued on its water-cooled mount. Placed in a vacuum of 10^{-6} mbar to suppress cooling through convection, we performed a four-terminal measurement of the resistance with a current of about 100 mA, which is sufficiently low to neglect the increase in resistance due to ohmic heating. The four terminals were connected to the outside of the vacuum feedthrough so the measured values include in-vacuum connection leads and wire bonds. Table 3.1 shows both calculated and measured resistances of the chip wires. The measured values are systematically larger than the calculated ones. We attribute the difference to the additional resistance of the leads and wire bonds. With the real on-chip resistances about equal to the anticipated values the wires can carry enough current to produce the designed magnetic trapping potential.

3.5.3 Inter chip wire resistance

Additional measurements of the resistance between different chip wires was performed for two reasons.

(i) Since we did not fabricate a dedicated SiO_2 insulation layer on the silicon substrate, we have to check that the resistance between wires is still sufficiently large to avoid current leaking from one wire leaking into an other. This effect is undesirable as it modifies the magnetic trapping potential in an uncontrolled way. A measurement of the resistance gives an impression of the amount of current that leaks out of the wire and a measure for the anticipated deviations in the magnetic field.

(ii) Although we normally only consider magnetic manipulation of our trapped

atoms also electrostatic manipulation is possible (see Sec. 2.4). To produce the (large) electrostatic fields necessary chip wires need to be charged to typically several tens or hundreds of volts. Obviously this is only possible if the interwire resistance is sufficiently large.

We have measured the inter chip wire resistance using a digital multimeter with the chip mounted in vacuum both directly after fabrication and after three months of use in typical trapping and cooling experiments. The results are shown in Table 3.2. The resistances immediately after fabrication are approaching MΩ values. These values are too large to be explained be the resistivity of the silicon. We assume the resistance is mainly determined by the thin oxide layer (*native oxide*) that is present on all silicon surfaces exposed to air, possibly enhanced by the exposure to the oxygen plasma during fabrication [118,119]. The ratio between the wire and the interwire resistance approaches 10^{-6}, so naively one would expect a current leakage of only 10^{-6}, causing alterations to the magnetic trapping potential well below the mG level.

After three months of experiments the resistances had decreased significantly. We attribute the lowering of the resistance to diffusion of gold into the silicon oxide layer and maybe even into the silicon substrate. Gold is well-known for its diffusive properties [118]. The elevated temperatures caused by ohmic heating during experiments accelerate the diffusion process and indeed wire 5, which is used most intensively, has the lowest resistance with its neighbors. In the period following the second measurement of Table 3.2 the resistances appeared to not decrease any further, stabilizing at the listed values and these values are consistent with current experiments.

Also note that gold and rubidium form an alloy for mixtures with < 30 weight percent rubidium [120]. Squires [121] reports on attempts to employ a gold-rubidium alloy as a ^{87}Rb dispenser in a cold atom experiment. Such a dispenser would form a very clean source of rubidium and have the added advantage of being stable in air. Although the device was shown to work in principle, it was hampered by the low diffusion rate of Rb in gold.

3.5.4 Magnetic potential roughness

An important limitation of atom-chip-based magnetic potentials is the roughness associated with these potentials. It has been observed both in magnetic thin films chips [122] as well as in current-carrying wire chips. In wire chips it is caused by small angular deviations of the current flow in the wire. Since first observation of the effect [123–125], it has been studied extensively [114, 123, 126–135].

Normally the roughness of the potential is seen as a handicap as it hinders the flow of a BEC in the potential and breaks up a single cold cloud in several, ill-defined parts. Experimentalists have been looking for ways to reduce the potential roughness ever since the beginning of experiments with atom chips. The first improvement was the use of evaporation instead of electroplating as the technique to fabricate chip wires. The 50-nm grain size of evaporated wires (see Sec. 3.5.1) perturbs the current flow less than the >90-nm grain size of electroplated wires [130, 136]. Evaporation

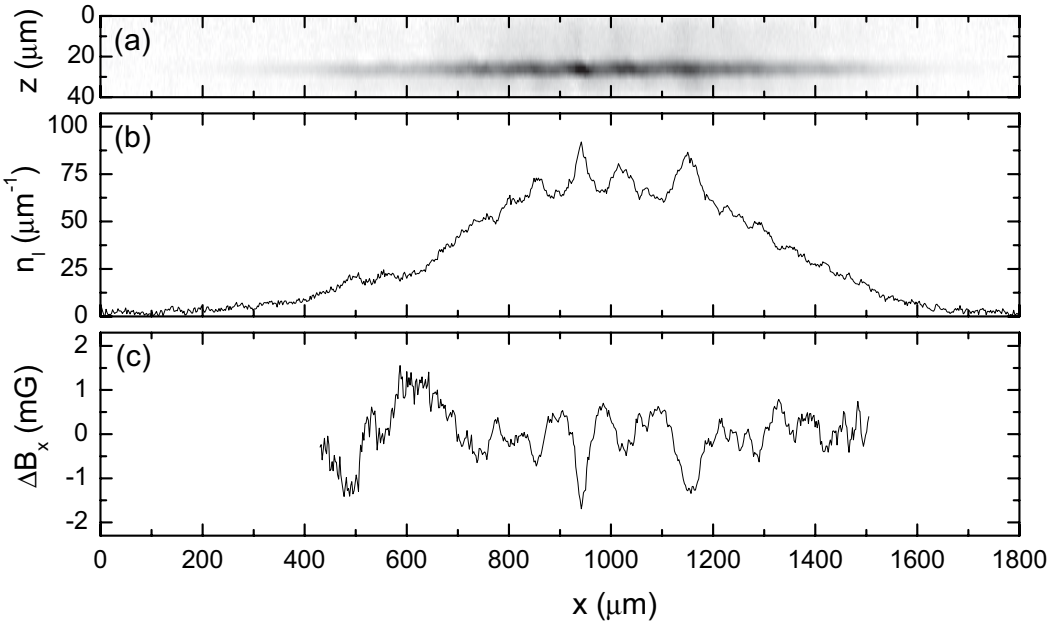

Figure 3.6: Initial characterization of potential roughness caused by wire corrugation. (a) Average of 50 *in-situ* images of a thermal cloud with a temperature of 0.35 μK. (b) The linear density extracted from (a). (c) The residual roughness of the potential expressed in mG after a harmonic fit representing the trapping field has been subtracted.

is currently the method of choice to make smooth chip wires.

Although potential roughness can be minimized using sophisticated microfabrication techniques and metal vapor deposition, there are also dynamic ways of compensating for residual potential roughness. Several methods have appeared in literature to suppress the effect. All these methods involve the use of non-static magnetic fields. Trebbia *et al.* [137] report on a suppression of the potential roughness with a factor 14 by modulating the wire current at a few tens of kHz. The bias field also has to be modulated. The limitations of this method are studied in [138]. Krüger *et al.* [133] propose a different method. Their idea is to add a rotating rf field orthogonal to the direction of the Ioffe field and then reduce the Ioffe field to zero since it is no longer necessary in the resulting time-orbiting potential (TOP). They predict a reduction of the potential roughness ΔB_x with a factor $\Delta B_x / b_{\mathrm{rf}}$. A third method for reducing the potential roughness was implemented as part of this thesis work and described in detail in Ch. 5. Linearly polarized radio-frequency fields can be used to create rf-dressed potentials in which the effect of the potential roughness is reduced with respect to the static potential. The exact reduction factor depends on the properties of the rf dressing.

Figure 3.6 shows how we did an initial characterization of the roughness of the potential generated by our main trapping wire. We loaded a thermal cloud containing $\sim 25 \times 10^3$ atoms into the potential formed by a current of 0.5 A in wire 5 (see Fig. 3.4) and a transverse bias field of 10.5 G. For these settings the distance between

atoms and the chip is ∼77 μm. After loading this trap we waited 500 ms to obtain an equilibrium density distribution which was subsequently measured through absorption imaging in the trap. We averaged 50 of these absorption images [Fig. 3.6(a)] to suppress imaging noise before computing the longitudinal density [Fig. 3.6(b)] using Eq. (2.36). The temperature of the thermal cloud was 0.35 μK, determined from the cloud width in time-of-flight. From the longitudinal density distribution we calculate the trapping potential using Eq. 2.36 . The roughness potential [Fig. 3.6(c)] is the residue of a parabolic fit to the potential. We express the roughness in a single number $\Delta B/B \approx 5 \times 10^{-5}$ which is the root mean square (rms) of the variations in Fig. 3.6(c) with $B = 10.5$ G.

This number is slightly larger than the one quoted in [88] for the very same wire. The difference can be explained from the difference in trapping height. It is a bit lower than the value of 7×10^{-5} in [133], although when we take into account that the latter was measured at only 5 μm from the chip, it becomes clear our wire does worse. The difference can not be explained from material properties or method of fabrication as in both cases it concerns a gold wire on a silicon substrate fabricated through optical lithography and gold evaporation.

The typical length scale is of the order of 100 μm, about the height of the atoms above the chip. The origin of the magnetic potential roughness is hard to infer from our microscopic analysis of the chip wires since variations in wire properties over this long length scale are practically impossible to detect.

3.5.5 Thermal properties

This section on the thermal properties of the atom chip deals with the way atom chip wires heat up when a large current is sent through them. This heating is an important effect that has to be taken into account because it determines the maximum allowable current in the chip wires.

To begin with, all heat in the chip wires is produced because of the resistivity of gold. At room temperature it has the value ρ_0=2.214 $\times 10^{-8}$ Ωm [139]. The temperature coefficient c is 3.6×10^{-3} K^{-1}, meaning that the temperature-dependent resistivity ρ_T can be approximated like

$$\rho_T = \rho_0 \left(1 + c\Delta T\right), \tag{3.3}$$

where ΔT is the deviation of the temperature from room temperature. This approximation is reasonable over a range of over 100 K. Generally the positive temperature coefficient is a nuisance as it increases the dissipation in the atom chip wires as they heat up while we try to keep the current constant. But we also use it to our advantage as it helps us to estimate the temperature rise in the wires. In practice we use

$$\Delta T = \frac{1}{c}\left(\frac{R}{R_0} - 1\right), \tag{3.4}$$

where R is the instantaneous resistance of a wire and R_0 the resistance of that wire at room temperature. The main limitation of Eq. (3.4) is in the assumption that the wire heats up uniformly which, given the varying width, is not the case.

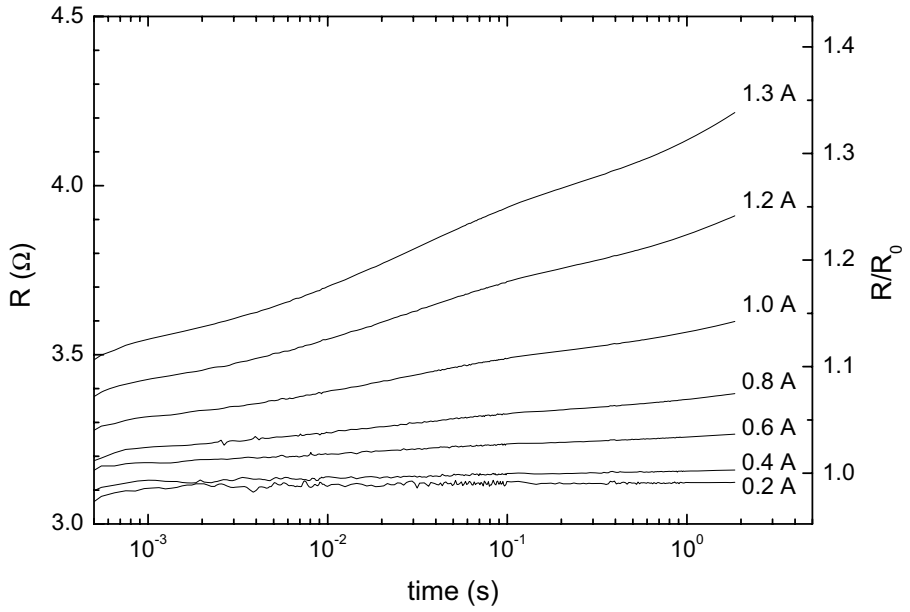

Figure 3.7: The resistance increase of chip wire 1 (10 μm wide) with increasing pulse duration. The different curves correspond to currents of 0.2 A, 0.4 A, 0.6 A, 0.8 A, 1.0 A, 1.2 A, and 1.3 A as indicated. Each curve is the average of 36 measurements.

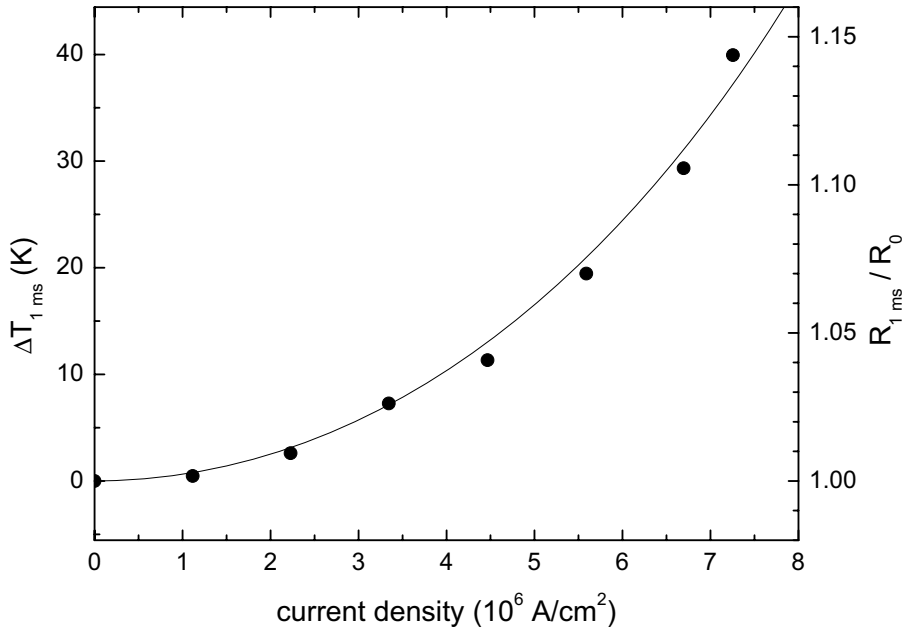

Figure 3.8: Heating of 10-μm-wide gold wire after 1 ms. The conductance to the substrate is used as fit parameter. The value found is $6.40 \pm 0.16 \times 10^6$ WK^{-1}m^{-2}.

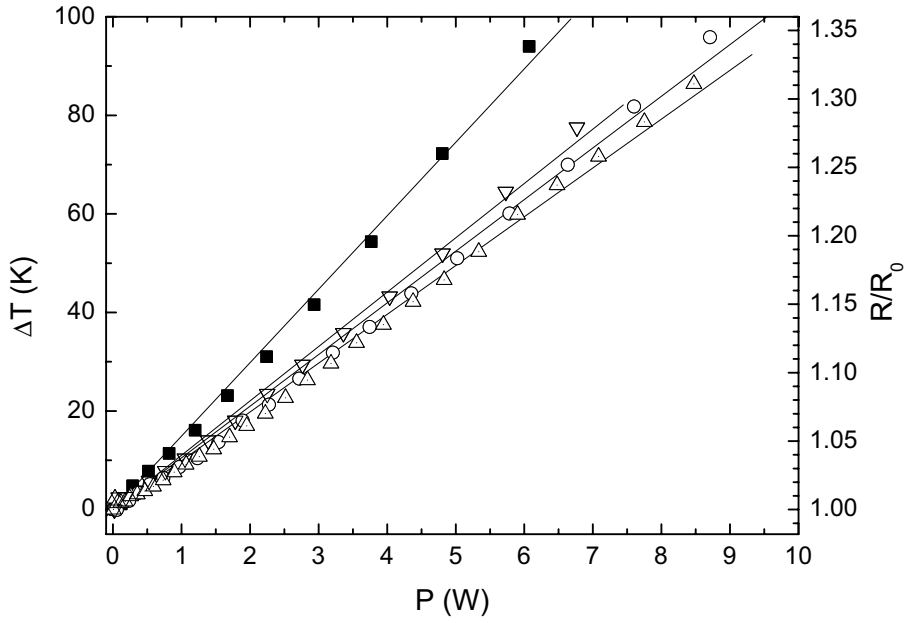

Figure 3.9: Temperature of four different chip wires against the power dissipated. The temperature is determined based on the resistance increase which is displayed on the right-hand axis. The measurement data is for chip wires 1 (■, 10 μm wide), 3 (○, 50 μm wide), 5 (△, 125 μm wide), and 7 (▽, 30 μm wide). The straight lines are linear fits to the data. The slopes are 14.9 ± 0.2, 10.5 ± 0.1, 9.90 ± 0.08, and 11.0 ± 0.1 K/W respectively.

In our experiments we limit the resistance increase to 30% which corresponds to a 83 K temperature rise. It will turn out (see Sec. 3.5.6) that this value is a good compromise between large current density on the one hand and safe distance from the melting point of gold (1337.58 K [139]) on the other.

We study the heating of the chip wires in two extremes. For very short current pulses we assume the silicon substrate to be a large heat sink absorbing all energy. Continuous operation of the chip wires is the other extreme. In the latter case the final chip wire temperature is determined by the total thermal resistance of the chip mount between the chip on top and the cooling water in the base of the mount. For current pulses of intermediate duration the way the chip wires heat up is more difficult to describe, because the different parts of the chip mount made of different materials and having different shapes influence the process (see also the discussion in Sec. 3.4 of [88]).

Following Groth *et al.* [62], the dissipation dP in a piece of wire with a length dl is

$$dP = \rho_0 \left(1 + c\Delta T\right) j^2 hwdl, \tag{3.5}$$

where j is the current density. This heat flows into the substrate or raises the temperature of the wire. Assuming a thermal conductivity k in between the wire and the substrate, the energy flow into the substrate is $k\Delta Twdl$; being only valid as long as the substrate is at room temperature. The increase of wire temperature

can now be described by the differential equation

$$\Delta\dot{T} = \frac{\rho_0 (1 + c\Delta T) hj^2 - k\Delta T}{h\rho C_p}, \tag{3.6}$$

with ρ the density and C_p the specific heat of the wire material. Assuming the temperature increase to be 0 at $t = 0$, the solution of the differential equation is

$$\Delta T(t) = \frac{h\rho_0 j^2}{k - hcj^2\rho_0} \left(1 - \exp^{-t/\tau}\right), \tag{3.7}$$

and the time constant τ equal

$$\tau = \frac{h\rho C_p}{k - hcj^2\rho_0}. \tag{3.8}$$

From this analysis we see that for $k - hcj^2\rho_0 \leq 0$ the temperature rises exponentially, destroying the wire immediately. For low currents the temperature saturates within microseconds for realistic numbers.

Figure 3.7 shows how the 10-μm-wide wire 1 (see Fig. 3.3) heats up for different currents*. After switch-on, the voltage over the wire needs almost 1 ms to stabilize, much longer than the time defined by τ in Eq. (3.8). We assume that 1 ms after switch-on the temperature difference between the wire and substrate has saturated and the substrate is still at room temperature. The resistance and temperature of the wire after 1 ms for the different currents is plotted in Fig. 3.8. As a fit function we use Eq. (3.7) with the exponential neglected and thermal conductance k as the fit parameter. This way we find a thermal conductance of $6.40 \pm 0.16 \times 10^6$ WK^{-1}m^{-2} which matches the value for 5-μm-wide gold wires on a silicon substrate with a 20-nm-thin SiO_2 insulation layer found in Ref. [62].

Figure 3.9 shows the temperature of several different wires on our chip as a function of the dissipated heat. For equal dissipation the temperature is lower for the wider wires showing that the thermal conductance calculated above does play a role, but the effect saturates for the broader wires. For these broader wires the thermal resistance between the silicon substrate and the base of the chip mount dominates (see also Table 3.3 of Ref. [88]). The slope of the curve of the 125-μm wire is 9.9±0.1 K/W.

In our experiments we use current pulses with a duration of 2 seconds or longer and a cycle time of 10 seconds. In most of our experiments we only use the 125-μm wire at high current, thus the continuous dissipation of the wire with a thermal resistance of 9.9 K/W is the best description for us.

3.5.6 Chip wire breakdown

In order to find the limitations in terms of current of our atom chips, a number of destructive tests were performed. Figure 3.10 shows the resistance of a wire of

*Note that R/R_0 can extend below 1 as R_0 is defined at room temperature and the wires are initially at somewhat lower temperature as the chip mount is water-cooled.

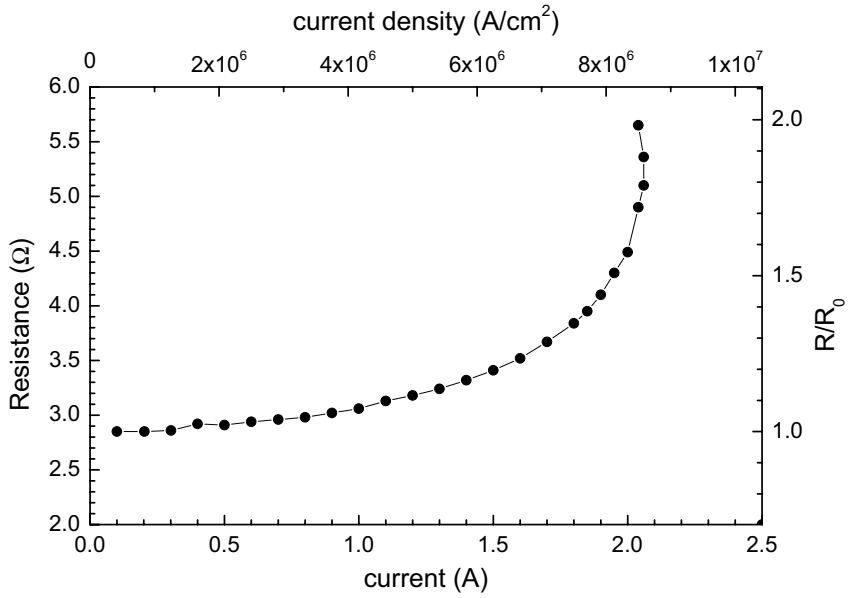

Figure 3.10: Resistance of a 20-μm-wide 1.2-μm-thick chip wire as voltage over the wire is increased. The resistance doubles before the wire fails at a current density of 8.6×10^6 A/cm^2.

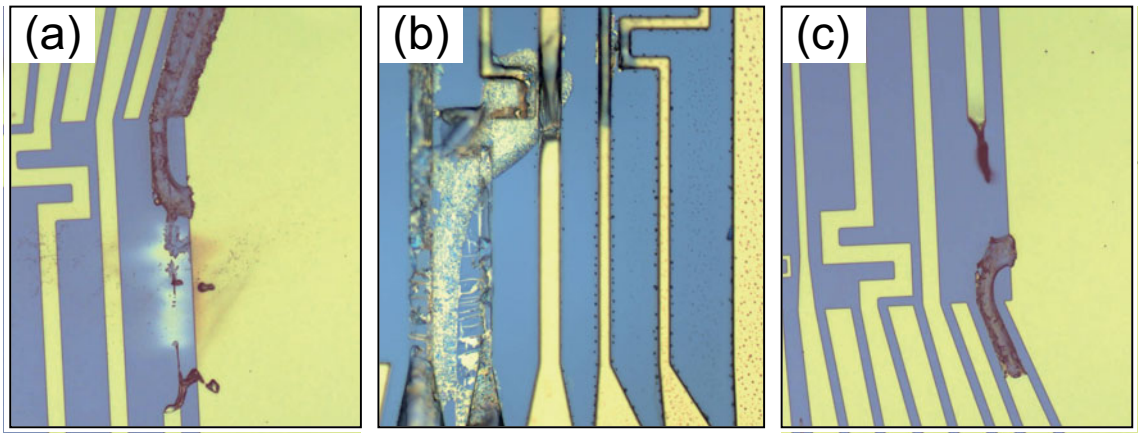

Figure 3.11: Three pictures showing what happens when chip wires overheat. (a) shows a wire that partially vaporized when it overheated. The vaporized gold re-deposited on the nearby substrate. In (b) several wires have melted after one of the wires has carried a large current for a long period (∼1 minute). The fact that several wires melted, shows that the substrate must have been very warm. The melted gold flowed over the substrate. (c) Apart from melting and vaporizing a wire may just peel of the substrate and break.

which the narrowest part is 20 μm wide, 1.3 mm long and 1.2 μm high as it is tested to destruction. The initial part of this measurement was performed with the power supply in constant-current mode, while the latter part had to be done with the supply in constant-voltage mode. The resistance doubles before the wire fails which appears typical behavior as it is similar to the results in [140].

The maximally achieved current density in this wire is 0.86×10^7 A/cm^2. For more narrow wires (down to 5 μm) we have observed values up to 1.1×10^7 A/cm^2. 10^7 A/cm^2 also is the typical number found in literature for the maximum current density in these wires [62, 141]. Only under special circumstances, like very narrow (sub-μm) wires [140] or cryogenically cooled chips [142], larger current densities are reported. From the measurement in Fig. 3.10 and similar measurements we conclude that our usual way of working in which we limit the resistance increase to 30% is very reasonable. At $R/R_0 = 1.3$ the current (density) is $> 80\%$ of the maximum value while the dissipation is still less than half the critical dissipation at the moment of failure.

Figure 3.11 shows three microscope images of chip wires that were destroyed by large currents. On close inspection of these images one sees that the wires can be destroyed in different ways depending on the current, duration and the microstructure. The wire can peel off the substrate [Fig. 3.11(c)]. This is probably due to the difference in the expansion coefficients of gold (14.2×10^{-6} K^{-1}) and silicon (3×10^{-6} K^{-1}) [143]. As soon as part of the wire loses contact with the substrate locally, its heat can no longer be transferred to the substrate and it overheats rapidly. Often parts of wires are seen to have melted. As soon as (part of) a wire melts it is destined to fail rapidly since the resistivity of liquid gold is 132% larger than that of solid gold [139]. Figure 3.11(b) shows an example of a molten wire. In this particular case the substrate must have been very hot since also parts of wires that were not carrying any current have melted. Finally it is possible that a wire (partially) vaporizes. This is what happened to the wire seen in Fig. 3.11(a). The gold is re-deposited on the silicon substrate nearby.

In all cases there is a large risk that one overheated wire will damage or short-circuit neighboring wires, independent of whether these wires are carrying current or not, consequently rendering the atom chip partially, or even completely, inoperable. Limiting the chip wire current to a maximum resistance increase of 30% has proven to be a reliable way to prevent such a catastrophe.

3.6 Summary and conclusion

In summary, we have given a detailed description of the fabrication procedure for our atom chips, and of the considerations that led to the choices made. The resulting atom chip wires were characterized using optical, electron and atomic force microscopy and their quality found to be competitive with the best chips reported thus far [140].

The fabrication procedure includes the use of optical lithography with a practical resolution of $\sim$3 μm, gold evaporation and lift off to fabricate gold wires with widths ranging from 5 to 125 μm and a typical thickness of 2 μm on a silicon substrate. With the chip epoxied to a water-cooled mount we achieve continuous current densities of $\geq 10^6$ A/cm^2 and $\geq 10^7$ A/cm^2 for the 125 μm and 5 μm wire, respectively, in ultra-high vacuum. Although we do not observe any particular problem in microscopic analysis of the microfabricated wires, they still exhibit the typical potential

roughness that is also observed in other atom chip experiments. In initial characterization experiments we found a rms value for $\Delta B/B$ of 5×10^{-5} at 77 μm above the chip, somewhat higher than chips fabricated in a similar way at other institutes. At least part of the explanation could be the native siliconoxide layer which presumably is only several nm thick and provides insufficient electrical insulation to prevent electrical current from leaking out of the wires.

Despite their limitations these chips have been successfully used to study the one-dimensional Bose gas [73] and to study atom-chip-based rf-dressed potentials [84], see also Ch. 5 and Ch. 6. The process described here was optimized for simplicity, and requires relatively modest clean-room facilities. It should thus particularly suited for reproduction elsewhere, employing similar facilities to those of the Amsterdam nanoCenter.

If in the near future new chips have to be made for a followup experiment, it is advisable to have a SiO_2 layer on the substrate to improve electrical insulation between the chip wires. A thin layer of 25 nm is reported to be sufficient [98], while it hardly obstructs the heat flow from the wire into the substrate [62]. It would only add one more stage to the fabrication process, thus keeping it relatively simple. An alternative would be to employ a dielectric substrate, doing away with the need for an insulating SiO_2 layer altogether. Industrial-grade polycrystalline AlN has a thermal conductivity in the 160–200 $Wm^{-1}K^{-1}$ range depending on the sintering process and possible additives. The thermal conductivity of monocrystalline AlN is larger, but limited by impurities, especially oxygen atoms. The largest value measured for a high-purity monocrystalline sample is 275 $Wm^{-1}K^{-1}$ [144]. AlN is used in the semiconductor industry as substrate and packaging material for power electronics. For our atom chip the monocrystalline variety would be preferred not only because of the larger thermal conductance, but also for its anticipated smaller surface roughness. One account of an AlN atom chip has appeared in literature [141]. Its thermal properties are favorable while the quality of the generated magnetic potential was not reported.