Schedulability Analysis of Global Scheduling for Multicore Systems With Shared Caches

Jun Xiao®, Member, IEEE, Sebastian Altmeyer, Member, IEEE, and Andy D. Pimentel®, Senior Member, IEEE

Abstract—Shared caches in multicore processors introduce serious difficulties in providing guarantees on the real-time properties of embedded software due to the interaction and the resulting contention in the shared caches. To address this problem, we develop a new schedulability analysis for real-time multicore systems with shared caches, globally scheduled by Earliest Deadline First (EDF) and Fixed Priority (FP) algorithms. We construct an integer programming formulation, which can be transformed to an integer linear programming formulation, to calculate an upper bound on cache interference exhibited by a task within a given execution window. Using the integer programming formulation, an iterative algorithm is presented to obtain the upper bound on cache interference a task may exhibit during one job execution. The upper bound on cache interference is subsequently integrated into the schedulability analysis to derive a new schedulability condition. A range of experiments is performed to investigate how the schedulability is degraded by shared cache interference. We also evaluate the schedulability performance of EDF against FP scheduling over randomly generated tasksets. Our empirical evaluations show that EDF is better than FP scheduling in terms of the number of task sets deemed schedulable.

Index Terms—Real-time systems, multi-core systems, schedulability analysis, shared caches, global scheduling

1 INTRODUCTION

MUlticore architectures are increasingly used in both the desktop and the embedded markets. Modern multicore processors incorporate shared resources between cores to improve performance and efficiency. Shared caches are among the most critical shared resources on multicore systems as they can efficiently bridge the performance gap between memory and processor speeds by backing up small private caches. However, this brings major difficulties in providing guarantees on real-time properties of embedded software due to the interaction and the resulting contention in a shared cache.

In a multicore processor with shared caches, a real-time task may suffer from two different kinds of cache interferences [1], which severely degrade the timing predictability of multicore systems. The first is called intra-core cache interference, which occurs within a core, when a task is preempted and its data is evicted from the cache by other real-time tasks. The second is inter-core cache interference, which happens when tasks executing on different cores access the shared cache simultaneously. Inter-core cache interference may cause several types of cache misses including capacity misses, conflict misses and so on [2]. In this work, we consider non-preemptive task systems, which implies that intra-core cache interference is avoided since no preemption is possible during task execution. We therefore focus on inter-core cache interference.

It is challenging to design real-time applications executing on multicore platforms with shared caches, which cannot afford to miss deadlines and hence demand timing predictability. Any schedulability analysis requires knowledge about the Worst-Case Execution Time (WCET) of real-time tasks. With a multicore system, the WCETs are strongly dependent on the amount of inter-core interference on shared hardware resources such as main memory, shared caches and interconnects. In this paper, we shall only focus on the shared cache interferences and study the schedulability analysis problem for hard real-time tasks that exhibit shared cache interferences.

A major obstacle is to predict the cache behavior to accurately obtain the WCET of a real-time task considering inter-core cache interference since different cache behaviors (cache hit or miss) will result in different execution times of each instruction. In [3], it was even pointed out that “it will be extremely difficult, if not impossible, to develop analysis methods that can accurately capture the contention among multiple cores in a shared cache”. In this paper, we assume that a task’s WCET itself does not account for shared cache interference but, instead, we determine this interference explicitly (as will be explained later on). [4] presents such an approach to derive a task’s WCET without considering shared cache interference.

This paper proposes a novel schedulability analysis of global real-time scheduling for multicore systems with shared caches. We construct an integer programming formulation, which can be transformed to an integer linear programming formulation, to calculate an upper bound on cache interference exhibited by a task within a given execution window. Using the integer programming formulation, an iterative
algorithm is presented to obtain the upper bound on cache interference a task may exhibit during one job execution. The upper bound on cache interference is subsequently integrated into the schedulability analysis to derive a new schedulability condition. A range of experiments is performed to investigate how the schedulability is degraded by shared cache interference for a range of different tasksets.

The original version of our schedulability analysis for real-time multicore systems with shared caches was presented in [5]. Significant extensions are made in this paper, including:

- A more general framework for the schedulability analysis of global scheduling, accounting for shared cache interference. The original scheduling analysis mainly focuses on FP scheduling, while the extended scheduling analysis presented in this work applies not only to FP scheduling but also to EDF scheduling;
- Evaluation of the schedulability performance of EDF against FP scheduling over randomly generated tasksets. Our empirical evaluations show that EDF is slightly better than FP scheduling in terms of task sets deemed schedulable.

The rest of the paper is organized as follows. Section 2 gives an overview of the related work. The system model is described in Section 3. Section 4 describes the proposed schedulability analysis, where we also detail the computation of processor-contention and inter-core cache interferences applied in the analysis. Section 5 presents an iterative computation to obtain the upper bound of inter-core cache interferences. Section 6 presents the experimental results, after which Section 7 concludes the paper.

2 RELATED WORK

**WCET Estimation.** For hard real-time systems, it is essential to obtain each real-time task’s WCET, which provides the basis for the schedulability analysis. WCET analysis has been actively investigated in the last two decades, of which an excellent overview can be found in [6]. There are well-developed techniques to estimate real-time tasks’ WCET for single processor systems. Unfortunately, the existing techniques for single processor platforms are not applicable to multicores with shared caches. Only a few methods have been developed to estimate task WCETs for multicore systems with shared caches [7], [8], [9]. In almost all those works, due to the assumption that cache interferences can occur at any program point, WCET analysis will be extremely pessimistic, especially when the system contains many cores and tasks. An overestimated WCET is not useful as it degrades system schedulability.

**Shared Cache Interference.** Since shared caches considerably complicate the task of accurately estimating the WCET, many researchers in the real-time systems community have recognized and studied the problem of cache interference in order to use shared caches in a predictable manner. Cache partitioning, which isolates application workloads that interfere with each other by assigning separate shared cache partitions to individual tasks, is a successful and widely-used approach to address contention for shared caches in (real-time) multicore applications. There are two cache partitioning methods: software-based and hardware-based techniques [10]. The most common software-based cache partitioning technique is page coloring [11], [12], [13], [14]. By exploiting the virtual to physical page address translations present in virtual memory systems at OS-level, page addresses are mapped to predefined cache regions to avoid the overlap of cache spaces. While cache partitioning technique using page coloring has the following drawbacks. First, it requires heavy modifications to virtual memory subsystem in the operating system. Second, the number of partitions is limited as a cache partition is coarsely sized (multiples of page size \( \times \) cache ways). Hardware-based cache partitioning is achieved using a cache locking mechanism [3], [13], [15], which prevents cache lines from being evicted during program execution. For example, [16] presented vCAT, an approach for dynamic shared cache management on multicore virtualization platforms based on Intel’s Cache Allocation Technology (CAT). The drawback of cache locking is that it requires specific hardware support that is not available in many commercial processors. Cache way-partitioning like CAT has also significant limitation due to a small number of coarsely-sized partitions (in multiples of way size).

**Real-Time Scheduling.** The schedulability analysis of global multiprocessor scheduling has been intensively studied [17], [18], [19], [20], [21], [22], [23], of which comprehensive surveys can be found in [24], [25]. Most multi-core scheduling approaches assume that the WCETs are estimated in an offline and isolated manner and that WCET values are fixed.

A few works address schedulability analysis for multi-core systems with shared caches [26], [27], [28], but these works deployed cache partitioning techniques. Real-time scheduling for multi-core systems using cache partitioning techniques is done via two steps: it first captures the relationship between the task’s WCET and cache allocation by analysis or measurement as the WCET of a task depends on the number of cache partitions assigned to that task, and then develops a strategy that determines the number of cache partitions assigned to each task in the system, so that the task system is schedulable. Existing approaches typically adopt Mixed Integer Programming to find the optimal cache assignment. However, these methods incur a very high execution time complexity, and are therefore too inefficient to be practical [28].

Different from the above work, we developed a new schedulability analysis of global scheduling for multicore systems in which cache space isolation techniques are not deployed. Instead of using cache partitioning to eliminate shared cache interference, we focus on the analysis of shared cache interference that a task may exhibit during its execution. Our approach neither requires operating system modifications for page coloring nor hardware features for cache locking.

Our work also differs from other approaches to the timing verification of multicore systems [29] in that all other sources of interferences are assumed to be included within the WCET. We analyze the effect of shared cache interference on the schedulability. To the best of our knowledge, this is among the first works that integrates inter-core cache interference into schedulability analysis.

3 SYSTEM MODEL

3.1 Task Model

We consider a set \( \tau = \{ \tau_1, \tau_2, \ldots, \tau_n \} \) to be scheduled on a multicore processor. Each task \( \tau_k = (C_k, D_k, T_k) \in \tau \) is characterized by a worst-case
computation time \( C_k \), a period or minimum inter-arrival time \( T_k \), and a relative deadline \( D_k \). All tasks are considered to be deadline constrained, i.e., the task relative deadline is less or equal to the task period: \( D_k \leq T_k \).

We further assume that all those tasks are independent, i.e., they have no shared variables, no precedence constraints, and so on. Moreover, jobs of any task cannot be executed at the same time on more than one core. A task \( t_k \) is a sequence of jobs \( J_k^j \), where \( j \) is the job index. We denote the arrival time, starting time, finishing time and absolute deadline of a job \( j \) as \( r_k^j, s_k^j, f_k^j \) and \( d_k^j \) respectively. Note that the goal of a real-time scheduling algorithm is to guarantee that each job will complete before its absolute deadline: \( f_k^j \leq d_k^j = r_k^j + T_k \).

As explained, it is difficult to accurately estimate \( C_k \) considering cache interference of other tasks executing concurrently. It should be pointed out that \( C_k \) in this paper refers to the WCET of task \( k \), assuming task \( k \) is the only task executing on the multicore processor platform, i.e., any cache interference delays are not included in \( C_k \).

Since time measurement cannot be more precise than one tick of the system clock, all timing parameters and variables in this paper are assumed to be non-negative integer values.

### 3.2 Architecture Model

Our system architecture consists of a multicore processor with \( m \) identical cores onto which the individual tasks are scheduled. Most multicore processors have instruction and data caches. Caches are organized as a hierarchy of multiple cache levels to address the tradeoff between cache latency and hit rate. The low level caches (LL1) in our considered multicore processor are assumed to be private, while the last level caches (LLC, for example LL2) are shared between all cores. Furthermore, we assume that the LLC cache is non-inclusive with respect to the private caches (LL1), and that LLC caches are direct-mapped caches.

Data caches, in general, are hard to analyze statically. In this work, we focus on instruction caches and we adopt the approach in [4] to derive task WCET. The analysis would require further extension in order to be applied to data caches.

### 3.3 Global Schedulers

In this paper, we focus on non-preemptive global scheduling. Once a task instance starts execution, any preemption during the execution is not allowed, so it must run to completion. So we do not have to consider intra-core cache interference. If not explicitly stated, cache interference will therefore refer to inter-core cache interference in the following discussion. We consider two well-known global scheduling algorithms: Non-Preemptive Earliest Deadline First (EDF\(_{np}\)) and Non-Preemptive Fixed Priority (FP\(_{np}\)).

EDF\(_{np}\) assigns a priority to a job according to the absolute deadline of that job. A job with an earlier absolute deadline has higher priority than others with a later absolute deadline. Since each job’s absolute deadline changes over time, the priority of a task changes dynamically.

For FP\(_{np}\) scheduling, a fixed priority \( P_i \) is assigned to each task \( t_k \) \((k = 1, 2, \ldots, n)\). As each task has a unique priority, we use \( hp(k) \) to denote the set of tasks with higher priorities than \( t_k \), and \( lcp(k) = hp(k) \cup \{ t_k \} \) the set of tasks whose priorities are not lower than \( t_k \). Similarly, \( lp(k) \) is the set of tasks with lower priorities than \( t_k \) and \( lcp(k) = lp(k) \cup \{ t_k \} \) the set of tasks whose priorities are not higher than \( t_k \).

The EDF\(_{np}\) and FP\(_{np}\) scheduling algorithms are work-conserving, according to the following definition.

**Definition 1.** A scheduling algorithm is work-conserving if there are no idle cores when a ready task is waiting for execution.

### 4 Schedulability Analysis

In this section, we give an overview of the new schedulability analysis that accounts for cache interference. We also present the approaches to derive the upper bound on the parameters used in the schedulability condition.

#### 4.1 Overview

We first analyze the execution of one job \( J_k^j \) of a task \( t_k \). Let \( o_k^j \) denote the latest time-instant no later than \( r_k^j \) \((o_k^j \leq r_k^j)\) at which at least one processor is idle and let \( A_k = r_k^j - o_k^j \). As all processors are idle when the system starts, there always exists such a \( o_k^j \). The time interval \([o_k^j, d_k^j]\) can be divided into two parts \([o_k^j, s_k^j]\) and \([s_k^j, d_k^j]\).

As shown in Fig. 1, a job \( J_k^j \) of task \( t_k \) exhibits two kinds of interferences during \([o_k^j, d_k^j]\). The first interference is called processor-contention interference, denoted by \( I_{pre}^{pre} \). It is the cumulative length of all intervals over \([o_k^j, s_k^j]\) in which all the processing cores are busy executing jobs other than \( J_k^j \).

We define the interference \( I_{pre}^{pre} \) of a task \( t_k \) on a task \( t_i \) over the interval \([o_k^j, s_k^j]\) as the cumulative length of all intervals in which \( t_i \) is executing. The second type of interference is the cumulative length of all extra execution delays caused by shared cache interference from all other tasks running concurrently on other cores, denoted as \( I_{sc}^{pre} \). We also define the interference \( I_{pre}^{pre}^{sc} \) as the cumulative length of all extra execution delays of \( t_k \) caused by shared cache accesses between task \( t_i \) and task \( t_k \).

Furthermore, we define the upper bound on processor-contention interference as \( I_{pre}^{pre} \) and similarly the upper bound on shared cache interference as \( I_{pre}^{sc} \).

Note that the processor-contention interference \( I_{pre}^{pre} \) occurs during \([o_k^j, s_k^j]\), so \( I_{pre}^{pre} \) depends on \( A_k \) and the length of \([r_k^j, s_k^j]\). While the shared cache interference \( I_{sc}^{pre} \) occurs only during \( t_k \)'s execution. We will present the derivation of \( I_k^{pre} \) in the next section and it can be shown that \( I_k^{pre} \) does not depend
on \( A_k \) and the length of \( [r_k^i, s_k^i] \). Let us now assume \( I_k^{ce} \) is known.

We can compute the latest start time of job \( J_k^i \) from task \( t_k: t_k^i = d_k^i - C_k - I_k^{ce} \) i.e., if \( J_k^i \) starts its execution before \( t_k^i \), it will be able to finish execution before deadline \( d_k^i \). The length of \( [r_k^i, t_k^i] \) is \( S_k = D_k - C_k - I_k^{ce} \). Since we consider non-preemptive scheduling, in order for \( J_k^i \) to miss its deadline, all \( m \) cores must be continuously busy executing tasks other than \( t_k \) in the time interval \( [o_k^i, t_k^i] \). In other words, if \( S_k < 0 \), \( J_k^i \) will miss its deadline. Therefore, we name the time interval \( [o_k^i, t_k^i] \) as a problem window. We assume \( S_k \geq 0 \) in the following description.

As the processor-contention interference only occurs before the start of the \( t_k \)'s execution, we restrict \( I_k^{pre}, I_k^{pre} \) and \( I_k^{ce} \) to the time interval \( [o_k^i, t_k^i] \).

By construction, we have the first schedulability test for \( t \).

\[ \text{Theorem 1. A task set } \tau \text{ is schedulable with a } EDF_{np} \text{ or } FP_{np} \text{ scheduling policy on a multicore processor composed of } m \text{ identical cores with shared caches if for each task } t_k \in \tau \text{ and all } A_k \geq 0 \]

\[ \bar{I_k}^{pre} + C_k + I_k^{ce} < D_k + A_k. \]

4.2 Computation of \( I_k^{pre} \)

The workload \( W_{i,k} \) of a task \( t_i \) is the time task \( t_i \) executes during time interval \( [o_k^i, t_k^i] \) of length \( A_k + S_k \), according to a given scheduling policy.

\[ \text{Lemma 1. The processor-contention interference that a task } t_i \text{ causes on a task } t_k \text{ in } [o_k^i, t_k^i] \text{ is never greater than the workload of } t_i \text{ in } [o_k^i, t_k^i] \]

\[ \forall i, k, j \quad I_{i,k}^{pre} \leq W_{i,k}. \]

Lemma 1 is obvious, since \( W_{i,k} \) is an upper bound on the execution of \( t_i \) in \( [o_k^i, t_k^i] \).

Note that \( t_i \) may execute more than \( C_i \) due to the shared cache interference. That is, the actual execution time of \( t_i \)'s job is bounded by \( C_i' = C_i + I_k^{ce} \). In the following discussion, we use \( C_i' \) as the upper bound on the workload contribution from a single job of \( t_i \).

As the number of \( t_i \)'s jobs released in \( [o_k^i, t_k^i] \) is at most \( \left\lfloor \frac{A_k + S_k}{T_i} \right\rfloor \), \( W_{i,k} \) can be roughly bounded by \( \left\lfloor \frac{A_k + S_k}{T_i} \right\rfloor \times C_i' \).

However, a tighter upper bound on the worst-case workload can be calculated by categorizing each job of \( t_i \) in \( [o_k^i, t_k^i] \) into one of the three types [30]:

- **carry-job**: a job with its release time earlier than \( o_k^i \) but with its deadline earlier than \( t_k^i \);
- **body-job**: a job with both its release time and its deadline in \( [o_k^i, t_k^i] \);
- **carry-out-job**: a job with its release time in \( [o_k^i, t_k^i] \), but with its deadline later than \( t_k^i \).

Fig. 4. The densest possible packing of jobs of \( t_i \) without carry-in job, if \( i = k \).

As shown in Fig. 2, the worst-case workload of \( t_i \) occurs when a carry-in job (if \( t_i \) has a carry-in job) finishes execution as late as possible and a carry-out job starts its execution as early as possible. We use \( W_{i,k}^{\alpha} \) to denote an upper bound of \( t_i \)'s workload in \( [o_k^i, t_k^i] \) if \( t_i \) has no carry-in job, and use \( W_{i,k}^{\alpha} \) to denote an upper bound of \( t_i \)'s workload if \( t_i \) has a carry-in job.

Following the approach in [19], we derive a tighter upper bound on \( W_{i,k}^{\alpha} \) and \( W_{i,k}^{\alpha} \) for the \( EDF_{np} \) and \( FP_{np} \) scheduling policies, separately. We omit the proof due to space limitations. Interested readers can refer to [19] for a detailed explanation.

4.2.1 Upper Bound on \( W_{i,k}^{\alpha} \) for \( EDF_{np} \)

\( EDF_{np} \) assigns a priority of a job by the absolute deadline of that job. We have the following lemma.

\[ \text{Lemma 2. For } EDF_{np}, \text{ if } D_i > D_k, \text{ the necessary condition for } J_k^i \text{ to cause interference to } J_k^j \text{ is } r_k^i < r_k^j, \text{i.e., } J_k^i \text{ must be released earlier than } J_k^j; \text{ if } D_i < D_k, \text{ the necessary condition for } J_k^i \text{ to cause interference to } J_k^j \text{ is } d_k \leq d_k, \text{i.e., } J_k^i \text{’s absolute deadline must be no later than that of } J_k^j. \]

\[ \text{Proof. Lemma 2 is from [19]. See the proof of Lemma 2 in [19].} \]

Since \( t_i \) has no carry-in jobs in this case, the worst case of \( W_{i,k}^{\alpha} \) occurs when the first job of \( t_i \) is released at time \( o_k^i \). The next jobs of \( t_i \) are then released periodically every \( T_i \) time units. Thus, \( W_{i,k}^{\alpha} \) is computed by three cases: (1) \( i = k \), (2) \( D_i \leq D_k \), (3) \( D_i > D_k \).

\[ 1) \quad i = k. \text{ As shown in Fig. 3, only body jobs in } [o_k^i, r_k^i], \text{ contribute to processor-contention interference and the number of } t_i \text{’s body instances is } \left\lfloor \frac{A_k}{T_i} \right\rfloor. \text{ So we have} \]

\[ W_{i,k}^{\alpha} = \left[ \frac{A_k}{T_k} \right] C_k'. \]

\[ 2) \quad D_i \leq D_k. \text{ Fig. 4 shows the worst case of } W_{i,k}^{\alpha} \text{ for } D_i \leq D_k. \text{ The number of body jobs of } t_i \text{ is } \left\lfloor \frac{A_k + S_k}{T_i} \right\rfloor. \]

Fig. 3. The densest possible packing of jobs of \( t_i \) without carry-in job, if \( i = k \).
We use $\alpha$ to denote the distance between $o_i^k$ and the deadline of $\tau_i$’s carry-out job, $\alpha = \frac{A_k + S_k}{T_i} T_i + D_k$. The deadline of $\tau_i$’s carry-out job is $o_i^k + \alpha$.

(2.A) If $\alpha \leq A_k + D_k$, as shown in case (a) in Fig. 4, the contribution of the carry-out job is bounded by $\min(C_i^*, (A_k + S_k) \mod T_i)$. In this case, we have

$$W_{i,k}^{n_3} = \left[ \frac{A_k + S_k}{T_i} \right] C_i^* + \min(C_i^*, (A_k + S_k) \mod T_i).$$  \hfill (2)

(2.B) If $\alpha > A_k + D_k$, shown as case (b) in Fig. 4, the contribution of the carry-out job is 0, we have

$$W_{i,k}^{n_3} = \left[ \frac{A_k + S_k}{T_i} \right] C_i^*.$$

\hfill (3)

3) $D_i > D_k$. Fig. 5 shows the worst case of $W_{i,k}^{n_3}$ for $D_i > D_k$. The number of body jobs of $\tau_i$ is $\left[ \frac{A_k + S_k}{T_i} \right]$. By Lemma 2, a job of $\tau_i$ can interfere with $J_k$ only if its release time is earlier than $r_i^k$. We use $\beta$ to denote the distance between $o_i^k$ and the release time of $\tau_i$’s carry-out job, $\beta = \left[ \frac{A_k + S_k}{T_i} \right] T_i$.

(3.A) If $A_k = 0$, then $o_i^k = r_i^k$. Since $D_i > D_k$, any task instance released no earlier than $o_i^k$ has a deadline later than $d_i^k$, so, $W_{i,k}^{n_3} = 0$.

(3.B) If $\beta < A_k$, shown as case (a) in Fig. 5. The contribution of $\tau_i$’s carry-out job is bounded by $\min(C_i^*, (A_k + S_k) \mod T_i)$. $W_{i,k}^{n_3}$ is computed by Equation (2).

(3.C) If $\beta \geq A_k > 0$, as shown in Fig. 5 case (b), the contribution of $\tau_i$’s carry-out job is 0, and $W_{i,k}^{n_3}$ is computed by Equation (3).

By the discussions above, we can compute $W_{i,k}^{n_3}$ for $EDF_{np}$ by

$$W_{i,k}^{n_3} = \begin{cases} 0 & D_i > D_k \land A_k = 0 \\ W_{i,k}^{n_1} & i = k \\ W_{i,k}^{n_2} & (i \neq k \land D_i \leq D_k \land \alpha < A_k + D_k), \\ W_{i,k}^{n_3} & \forall (D_i > D_k \land \beta < A_k) \\ W_{i,k}^{n_3} & \text{otherwise} \end{cases}$$

where $W_{i,k}^{n_1}$, $W_{i,k}^{n_2}$, $W_{i,k}^{n_3}$ are defined in Equations (1), (2) and (3) respectively.

### 4.2.2 Upper Bound on $W_{i,k}^{c}$ for $EDF_{np}$

We now compute the upper bound on $W_{i,k}^{c}$ for $EDF_{np}$ by four cases: (1) $i = k$, (2) $D_i \leq D_k$ and $S_i > C_i^*$ (3) $D_i > D_k$ and $S_i \geq C_i^*$ (4) the remaining cases.

1) $i = k$, shown in Fig. 6. The number of body jobs of $\tau_k$ is $\left[ \frac{A_k}{T_k} \right]$. The contribution of the carry-in job is bounded by $\min(C_i^*, \max(0, (A_k \mod T_k) - T_k + D_k))$. So in this case, we have

$$W_{i,k}^{c} = \left[ \frac{A_k}{T_k} \right] C_i^* + \min(C_i^*, \max(0, (A_k \mod T_k) - T_k + D_k)).$$

\hfill (5)

2) $D_i \leq D_k \land S_i > C_i^*$. Shown as case (a) in Fig. 7, the worst case of $W_{i,k}^{c}$ occurs when $\tau_i$’s last released instance has its deadline at $d_i^k$. The number of $\tau_i$’s body jobs is $\left[ \frac{A_k + D_k}{T_i} \right]$. The contribution of the carry-in job is bounded by $\min(C_i^*, (A_k + D_k) \mod T_i)$. So, we have

$$W_{i,k}^{c} = \left[ \frac{A_k + D_k}{T_i} \right] C_i^* + \min(C_i^*, (A_k + D_k) \mod T_i).$$

\hfill (6)

3) $D_i > D_k \land S_i \geq C_i^*$. Case (b) in Fig. 7 shows the worst case of $W_{i,k}^{c}$. By Lemma 2, $\tau_i$’s job can interfere with $J_k$ only if its release time is earlier than $r_i^k$. So, the worst case of $W_{i,k}^{c}$ occurs when one of $\tau_i$’s instances is released at $r_i^k - 1$.

(3.A) If $A_k > 0$, the number of $\tau_i$’s body instances is $\left[ \frac{A_k - 1}{T_i} \right]$, the carry-out is $C_i^*$, the carry-in is bounded by $\mu = \min(C_i^*, \max(0, (A_k - 1) \mod T_i - (T_i - D_i)))$.

(3.B) If $A_k = 0$, only the carry-out job contributes at most $C_i^* - 1$. So, we have

$$W_{i,k}^{c} = \begin{cases} C_i^* - 1 & A_k = 0 \\ \left( \left[ \frac{A_k - 1}{T_i} \right] + 1 \right) C_i^* + \mu & A_k > 0 \end{cases}$$

\hfill (7)

4) For the remaining cases, i.e., $(D_i \leq D_k \land S_i \leq C_i^*) \lor (D_i > D_k \land S_i < C_i^*)$, the worst case of $W_{i,k}^{c}$ occurs
Fig. 8. The densest possible packing of jobs of \( \tau_i \) with carry-in job. Case (a): \( D_i < D_k \land S_i < C_i^* \); case (b): \( D_i > D_k \land S_i < C_i^* \).

when one of \( \tau_i \)'s instances is released at \( t_i^k - C_i^{*} \), as shown in Fig. 8.

(4.A) If \( A_k + S_k \leq C_i^* \), then \( W_{i,k}^c = A_k + S_k \).

(4.B) If \( A_k + S_k > C_i^* \), the number of \( \tau_i \)'s body job is \( \left[ \frac{A_k + S_k - C_i^*}{T_i} \right] \), the contribution of the carry-out job is \( C_i^{*} \), carry-in is bounded by \( v = \min(C_i^{*}, \max(0, (A_k + S_k - C_i^{*}) \mod T_i - (T_i - D_i))) \)

\[
W_{i,k}^{c,i} = \left\{ \begin{array}{ll}
A_k + S_k & A_k + S_k \leq C_i^* \\
\left[ \frac{A_k + S_k - C_i^*}{T_i} \right] + 1 & A_k + S_k > C_i^* \\
\end{array} \right.
\]

By the discussion above, we can compute \( W_{i,k}^c \) for \( EDF_{np} \) by

\[
W_{i,k}^c = \left\{ \begin{array}{ll}
W_{i,k}^{c,i} & i = k \\
W_{i,k}^{c,i} & i \neq k \land D_i \leq D_k \land S_i > C_i^* \\
W_{i,k}^{c,i} & D_i > D_k \land S_i \geq C_i^* \\
W_{i,k}^{c,i} & \text{otherwise} \\
\end{array} \right.
\]

where \( W_{i,k}^{c,i}, W_{i,k}^{c,i}, W_{i,k}^{c,i} \) and \( W_{i,k}^{c,i} \) are defined in Equations (5), (6), (7) and (8) respectively.

4.2.3 Upper Bound on \( W_{i,k}^c \) for \( FP_{np} \)

The following lemma describes the condition of processor-contention interference on \( \tau_k \) caused by lower-priority tasks in \( lp(k) \) for \( FP_{np} \).

Lemma 3. For \( FP_{np} \), a task instance \( J_{p,i}^j \) of \( \tau_i \in lp(k) \) can interfere with \( J_{p,i}^j \) only if \( J_{p,i}^j \) is released before \( r_{i,j}^k \).

We compute the upper bound on \( W_{i,j}^n \) by three cases: (1) \( i = k \), (2) \( \tau_i \in lp(k) \), (3) \( \tau_i \in lp(k) \).

1) \( i = k \). The worst-case workload is the same as in the case of \( EDF_{np} \) thus \( W_{i,j}^n \) can be computed by Equation (1).

2) \( \tau_i \in lp(k) \). The worst-case workload of task \( \tau_i \) occurs when a job of \( \tau_i \) arrives at \( o_{i,j}^k \), as shown in case (a) in Fig. 4. \( W_{i,j}^n \) can be computed using Equation (2).

3) \( \tau_i \in lp(k) \). The worse case of \( W_{i,j}^n \) occurs when one of \( \tau_i \)'s instances is released at \( o_{i,j}^k \). The number of body jobs of \( \tau_i \) is \( \left[ \frac{A_k + S_k}{T_i} \right] \). Let \( \gamma \) be the distance between \( o_{i,j}^k \) and the release time of \( \tau_i \)'s last instance. So \( \gamma = \left[ \frac{A_k + S_k}{T_i} \right] \).

(3.A) If \( A_k = 0 \), then \( o_{i,j}^k = r_{i,j}^k \), according to Lemma 3, \( W_{i,j}^n \) is 0.

(3.B) If \( \gamma < A_k \), \( \tau_i \)'s last job is released earlier than \( r_{i,j}^k \), as shown in Fig. 9 case (a), its contribution is bounded by \( \min(A_k + S_k \mod T_i, C_i^*) \). In this case, \( W_{i,j}^n \) is computed by Equation (2).

(3.C) If \( \gamma \geq A_k > 0 \), as shown in case (b) of Fig. 9, the contribution of the last released job of \( \tau_i \) is 0. In this case, \( W_{i,j}^n \) can be computed by Equation (3).

By the above discussion, we can compute \( W_{i,j}^c \) by

\[
W_{i,j}^c = \left\{ \begin{array}{ll}
0 & \tau_i \in lp(k) \land A_k = 0 \\
W_{i,j}^{c,i} & i = k \\
W_{i,j}^{c,i} & \tau_i \in lp(k) \land \tau_i \in lp(k) \land \gamma < A_k \\
W_{i,j}^{c,i} & \text{otherwise} \\
\end{array} \right.
\]

where \( W_{i,j}^{c,i}, W_{i,j}^{c,i}, W_{i,j}^{c,i} \) and \( W_{i,j}^{c,i} \) are defined in Equations (1), (2) and (3) respectively.

4.2.4 Upper Bound on \( W_{i,k}^{c,i} \) for \( FP_{np} \)

We compute the upper bound on \( W_{i,k}^c \) by three cases: (1) \( i = k \), (2) \( \tau_i \in lp(k) \land S_i \geq C_i^* \), (3) the remaining cases.

1) \( i = k \). The worst case of \( W_{i,k}^c \) occurs as it does for \( EDF_{np} \) and therefore \( W_{i,k}^c \) is computed by Equation (5).

2) \( \tau_i \in lp(k) \land S_i \geq C_i^* \). The worst case of \( W_{i,k}^c \) occurs when one of \( \tau_i \)'s job is released at \( r_{i,j}^k - 1 \), as shown in case (b) of Fig. 7. We can compute \( W_{i,j}^c \) by Equation (7).

3) The remaining cases, i.e., \( \tau_i \in lp(k) \lor \tau_i \in lp(k) \land C_i^* > S_i \). The worst-case workload of \( \tau_i \) is generated when one of \( \tau_i \)'s instances is released at time instance \( s_{i,k}^l - C_i^* \). Such a situation is depicted in Fig. 8. In this case, we can compute \( W_{i,j}^c \) by Equation (8).

By the above discussion, we compute \( W_{i,j}^c \) by

\[
W_{i,j}^c = \left\{ \begin{array}{ll}
W_{i,j}^{c,i} & i = k \\
W_{i,j}^{c,i} & \tau_i \in lp(k) \land S_i \geq C_i^* \\
W_{i,j}^{c,i} & \text{otherwise} \\
\end{array} \right.
\]

where \( W_{i,j}^{c,i}, W_{i,j}^{c,i}, W_{i,j}^{c,i} \) and \( W_{i,j}^{c,i} \) are defined in Equations (5), (7) and (8) respectively.

4.2.5 Upper Bound on \( t_{i,k}^{pre} \)

By the definition of \( o_{i,j}^k \), at least one core is idle at \( o_{i,j}^k \), therefore at most \( m - 1 \) tasks have carry-in jobs. The task set \( \tau \) can be partitioned into two subsets \( \tau' \) and \( \tau'' \) that include tasks with carry-in jobs and tasks without carry-in jobs, respectively. Now we define \( \Omega_k \) as the maximal value of the sum of all tasks’ workloads in \( o_{i,j}^k \) among all possible cases

\[
\Omega_k = \max \sum_{\tau_i \in \tau} W_{i,k}^{c,i}
\]

(12)
where \( \tau^a \) and \( \tau^c \) satisfy \( \tau^a \cup \tau^c = \tau \), \( \tau^a \cap \tau^c = \emptyset \) and \( |\tau^c| \leq m - 1 \).

By taking the maximum over the task set, \( \Omega_k \) describes an upper bound on the total worst-case workload in \( [\sigma_k, t_k] \). The complexity to compute \( \Omega_k \) is \( O(n) \), as explained in [18].

Since both \( EDF_{np} \) and \( FP_{np} \) are work-conserving, the processor-contention interference exhibited by \( \tau_k \) can be bounded by \( \frac{\Omega_k}{m} \). So, we have the following Lemma.

**Lemma 4.** If tasks are scheduled with an \( EDF_{np} \) or \( FP_{np} \) scheduling policy on a multicore processor composed of \( m \) identical cores with shared cache

\[
I_{k}^{pre} \leq \frac{\Omega_k}{m}.
\]

The pessimism of the analysis of upper bound on the processor-contention interference mainly comes from the assumption that every tasks take the their worst-case execution time and the computational loads are equally distributed to \( m \) cores.

### 4.3 Computation of \( \tilde{I}^{wc}_{k} \)

We first identify the maximum cache interference between two tasks and then we construct an integer programming formulation to calculate the upper bound on the shared cache interference exhibited by a task within an execution window.

#### 4.3.1 Cache Interference Between Two Tasks

We first analyze the cache interference during one job execution between \( t_k \) and \( t_i \). Let \( t_k \) be the interfered and \( t_i \) be the interfering task.

Following the approach in [4], we can obtain the WCET of a task by performing a Cache Access Classification (CAC) and Cache Hit/Miss Classification (CHMC) analysis for each instruction memory access at the private caches and the shared LLC cache separately.

**CAC and CHMC.** The CAC determines the possibility that an instruction being fetched from memory will access a certain cache level, and the access to a certain cache level can be Always (A), Uncertain (U) or Never (N). A reference \( r \) at a cache level \( L \) is considered as \( A \) if the access to \( r \) is always performed at cache level \( L \) and \( r \) is considered as \( N \) if the access to \( r \) is never performed at cache level \( L \), while the access is classified as \( U \) if it is not \( A \) nor \( N \). CHMC assigns a cache lookup result to each memory reference according to the cache states. As a result, a reference to a memory block of instructions can be classified as Always Hit (AH), Always Miss (AM) or Uncertain (U).

The CAC for a reference \( r \) at a cache level \( L \) depends on the results of CAC and CHMC of the reference \( r \) at the level \( L-1 \). Since we consider noninclusive caches, accesses to the private caches cannot be affected by tasks executing on other cores. Accesses classified as \( AM \) or \( U \) at the shared LLC cache will also not be affected by shared cache interferences, since they are already counted as misses in the WCET analysis.

We start the cache interference analysis by defining two concepts for cache blocks.

**Definition 2.** A Hit Block (HB) is a memory block whose access is classified as AH at the shared LLC cache.

**Definition 3.** A Conflicting Block (CB) is a memory block whose access is classified as \( A \) or \( U \) at the shared LLC cache.

HB and CB can be identified by the approach proposed in [4].

We use \( HB_k = \{m_{k,1}, m_{k,2}, \ldots, m_{k,p}\} \) to represent the set of HB for task \( t_k \) and use \( n_{i,x} (x = 1, 2, \ldots, p) \) to denote the number of \( m_{i,x} \)’s accesses that are classified as an AH at the LLC cache. Similarly, we define \( CB_i = \{m_{i,1}, m_{i,2}, \ldots, m_{i,q}\} \) as the set of CB for task \( t_i \) and denote \( n_{i,x} \) as the number of \( m_{i,x} \)’s accesses that are classified as \( A \) or \( U \) at the LLC cache. Note that \( HB_k \) and \( CB_i \) include the memory blocks that meet the requirement in every program path that may be taken by the task.

In our system architecture, cache interference occurs only at the shared LLC cache when a cache line used by \( t_k \) is evicted by \( t_i \) and consequently causing reload overhead for \( t_k \). A cache line that may cause cache interference for \( t_k \) needs to satisfy at least two conditions:

1. access to that cache line will result in a cache hit at the LLC cache in WCET analysis of \( t_k \).
2. the cache line may be used by \( t_i \).

From the above two conditions, we can analyze memory block accessing that may cause interference. The first condition implies that only accessing to \( HB_k \) may cause cache interference for \( t_k \), while the second condition indicates that accessing to \( CB_i \) by \( t_i \) may interfere with \( t_k \). Furthermore, cache interference occurs only if \( t_k \) accesses memory blocks in \( HB_k \) and \( t_i \) accesses memory blocks in \( CB_i \) concurrently, and those memory blocks have the same cache index.

We use \( I_{k}^{wc} \) to represent the upper bound on the shared cache interference imposed on \( t_k \) by only one job execution of \( t_i \).

Suppose the indexes of the LLC cache range from 0 to \( N-1 \), we can derive \( N \) subsets of \( HB_k \) according to the mapping function \( idx \) that maps a memory address to the cache line index at the LLC cache as follows:

\[
m_{k,u} = \{m_{k,x} \in HB_k | idx(m_{k,x}) = u\}, (0 \leq u < N, u \in N).
\]

We define the characteristic function of a set \( A \) which indicates membership of an element \( x \) in \( A \) as

\[
\chi_A(x) = \begin{cases} 1 & x \in A \\ 0 & \text{otherwise} \end{cases}.
\]

Let \( N_{k,u} \) represent the number of hit accesses to the \( u \)th cache line by \( t_k \) without cache interference. \( N_{k,u} \) equals to the total number of access to the HBs mapping to the \( k \)th cache line

\[
N_{k,u} = \sum_{x=1}^{p} n_{k,x} \chi_{HB_k}(m_{k,x}).
\]

Similarly, we divide \( CB_i \) into \( N \) subsets by

\[
\hat{e}_{i,u} = \{m_{i,x} \in CB_i | idx(m_{i,x}) = u\}, (0 \leq u < N, u \in N).
\]

The number of accesses to the \( k \)th cache line by \( t_i \) is bounded by

\[
N_{i,u} = \sum_{x=1}^{q} n_{i,x} \chi_{CB_i}(m_{i,x}).
\]
Cache interference can only happen among memory blocks that are in the same subset that maps to the same cache line. For the $i$th cache line, $t_k$ can be interfered at most $N_{i,u}$ times and $t_r$ can interfere at most $N_{i,u}$ times. The following formula gives an upper bound on the number of cache misses by accessing the HBs for task $t_k$

\[ S(t_r, t_k) = \sum_{i=0}^{N-1} \min(N_{i,u}, N_{k,u}). \]

Suppose the penalty for an LLC cache miss is a constant, $C_{miss}$, then $I_{sc}^k$ can be calculated by

\[ I_{sc}^k = S(t_r, t_k)C_{miss}. \]

**Lemma 5.** The shared cache interference imposed on $t_k$ by only one job execution of $t_r$ can be bounded and $I_{sc}^k = S(t_r, t_k)C_{miss}$.

**Proof.** The lemma holds as discussed above. \(\square\)

The computation of $I_{sc}^k$ only takes the memory accesses of $t_k$ and $t_r$ as input, so $I_{sc}^k$ only depends on memory accesses of $t_k$ and $t_r$. Given a taskset, $I_{sc}^k$ can be computed. In the following discussion, we assume $I_{sc}^k$ is known.

Lemma 5 gives an upper bound on cache interference for $t_k$ imposed by only one job of $t_r$. It is possible that more than one job of $t_r$ interfere with $t_k$. We denote the number of jobs of $t_r$ that interfere with $t_k$ as $N_{i,k}$.

**Lemma 6.** The total cache interference $I_{sc}^k$ exhibited from $N_{i,k}$ jobs of $t_r$ is bounded by $N_{i,k}I_{sc}^k$.

**Proof.** For $N_{i,k}$ jobs of $t_r$, the total number of accesses to each memory block $m_{i,z}$ is bounded by $N_{i,k}m_{i,z}$. Thus, the execution of $N_{i,k}$ jobs of $t_r$ accesses the $k$th cache line also at most $N_{i,k}N_{i,u}$ times. From the proof of Lemma 5, the upper bound of the total cache interference exhibited by $t_k$ from $N_{i,k}$ jobs of $t_r$ is $\sum_{i=0}^{N-1} \min(N_{i,k}N_{i,u}, N_{k,u})C_{miss}$

\[ N_{i,k}I_{sc}^k = N_{i,k} \sum_{i=0}^{N-1} \min(N_{i,u}, N_{k,u})C_{miss} \]

\[ = \sum_{u=0}^{N-1} \min(N_{i,k}N_{i,u}, N_{i,k}N_{k,u})C_{miss} \]

\[ \geq \sum_{i=0}^{N-1} \min(N_{i,k}N_{i,u}, N_{k,u})C_{miss}. \]

\(\square\)

### 4.3.2 IP Formulation

We can compute an upper bound of the maximum cache interference a task may exhibit during an execution window by introducing an Integer Programming (IP) formulation, which can be transformed to an integer linear programming formulation.

It is necessary to check the schedulability of the task-set without considering cache interference. If the task-set does not pass the initial schedulability test, there is no need to calculate the cache interference. Only if all tasks (including $t_r$) pass the schedulability test (without considering cache interference), the IP is solved to compute the upper bound on cache interference. Therefore, the IP formulation is based on the assumption that $t_r$ is schedulable without cache interference.

If $N_{i,k}$ jobs of $t_r$ are executing concurrently with $t_k$, the cache interference that $t_k$ causes on $t_r$ is bounded by $N_{i,k}I_{sc}^k$ according to Lemma 6. As a task may exhibit cache interference from more than one task during a job execution, the total cache interference for one job execution of $t_k$ is bounded by the sum of the contributions of all other tasks $t_i(i \neq k)$ in the task set $\tau$. Thus, the objective function of the IP formulation is

\[ \max \sum_{i \neq k} N_{i,k}I_{sc}^k. \]

The IP formulation will have an unbounded solution without further constraints to the variable $N_{i,k}$. To get a bounded solution, we analyze the constraints on $N_{i,k}$. First, we define the concept of the execution window of a job.

**Definition 4.** The Execution Window (EW) of the $j$th job of $t_k$ ($J_j^k$) is time interval $[s_k^j, f_k^j]$ from the staring time to the finishing time of $J_j^k$.

Note that the length of an execution window may be larger than $C_i$, since the EW includes the cache interference. We use $C_{i,sc}$ as the length of the EW because of the iterative computation which will be described later on.

$N_{i,k}$ reaches its minimal value when a job of $t_r$ starts to execute as soon as it is released and the execution finishes just before the start of the EW, as shown the case (a) in Fig. 10. Denoting $C_{i,sc}^{min}$ as the smallest execution time of $t_r$, often called Best-Case Execution Time (BCET), we have the following constraint:

\[ \forall i \neq k, \left[ \frac{\max(0, C_{i,sc}^{\min} - T_i + C_{i,sc}^{\min})}{T_i} \right] + \xi_i \leq N_{i,k}, \]

(14)

where $\xi_i = \begin{cases} 1 & (C_k^i + C_{i,sc}^{\min}) \mod T_i - D_i < C_{i,sc}^{\min} \leq 0 \\ 0 & \text{otherwise} \end{cases}$

The term $\xi_i$ indicates whether the last job of $t_r$, released within the EW will interfere with $t_k$, since the last released job should start its execution $C_{i,sc}^{\min}$ before its relative deadline if the task is schedulable.

The maximum value of $N_{i,k}$ is taken when the first interfering job of $t_r$ finishes just after the start of the EW and the last interfering job of $t_r$ starts to execute at the time when it is released. Such a situation is depicted as case (b) in Fig. 10. Thus, we have the second constraint on $N_{i,k}$

\[ \forall i \neq k, N_{i,k} \leq 1 + \frac{\left[ \max(0, C_{i,k}^i - T_i + D_i) \right]}{T_i}. \]

(15)

If $N_{i,k} > 2$, the first and last interfering jobs of $t_r$ may occupy almost 0 computation capacity in the EW. Let $J_j$ be

![Fig. 10. Situations where $t_r$ interferes $t_k$ with the most and least number of jobs.](image-url)

Authorized licensed use limited to: Universiteit van Amsterdam. Downloaded on October 22,2020 at 16:17:27 UTC from IEEE Xplore. Restrictions apply.
such a job among the remaining $N_{i,k} - 2$ interfering jobs of $\tau_k$ between the first and the last ones. Both release time $r_i^t$ and deadline $d_i^t$ of $\tau_j$ are within the EW of $\tau_k$.

**Lemma 7.** If $\tau_i$ is schedulable without considering cache interference, $C_i$ computation capacity of the processing core is reserved for the execution of $j_i^l$ during $[r_i^l, d_i^l]$. If $j_i^l$ executes for $C_{i^l} < C_i$, the processing core will be accumulatively idle (executing nothing, simply wasting the processing capacity for $\tau_i$) for at least $C_i - C_{i^l}$ during $[r_i^l, d_i^l]$.

**Proof.** If $\tau_i$ satisfies the schedulability condition without considering cache interference: $\frac{\gi}{m} + C_i < D_i$, the core on which $j_i^l$ is executed spends at most $D_i - C_i$ in total for the execution of other interfering tasks during $[r_i^l, d_i^l]$. $j_i^l$ is guaranteed to have $C_i$ computation capacity during $[r_i^l, d_i^l]$.

The remaining computation capacity of a multicore processor with $m$ cores is $(m - 1)C_k^\prime$ since one core is dedicated to the execution of $\tau_k$. Due to the limited computation capacity of the processor, the total execution of the tasks that may interfere with $\tau_k$ within the EW cannot exceed $(m - 1)C_k^\prime$.

Hence, we have the third constraint

$$\sum_{i \neq k} \max(0, N_{i,k} - 2)C_i \leq (m - 1)C_k^\prime. \quad (16)$$

The objective function (13) together with three constraints on $N_{i,k}$, i.e., inequalities (14), (15) and (16), form our IP problem. Since $C_{i^\text{min}}$ is a relatively small number, we take the extreme case: $C_{i^\text{min}} = 0$. As task parameters such as $C_i, D_i, T_i$ are known, the optimal solution of the IP only depends on the length of $EW$. Thus, we use $I^*(C_k^\prime)$ to denote the optimal value of the IP problem if $C_k^\prime$ is used as the length of the $EW$ in the IP.

Note that inequalities (14) and (16) are based on the assumption that $\tau_i$ is schedulable. Thus, before solving the IP, we have to check the schedulability of the taskset assuming no cache interference between tasks, i.e., $I^* = 0$.

**Computation Complexity of the IP.** The original IP can be easily transformed to an Integer Linear Programming (ILP) problem by introducing a new integer variable $y_{i,j}$ for each $N_{i,j}$ with two additional constraints: $y_{i,j} \geq 0$ and $y_{i,j} \geq N_{i,k} - 2$. Inequality (16) can be replaced by $\sum_{i \neq k} y_{i,k}C_i \leq (m - 1)C_k^\prime$. In the transformed ILP problem, we have totally $2(n - 1)$ variables and $4(n - 1) + 1$ constraints. The complexity of the IP is the same as the complexity of solving the transformed ILP problem, which is $O(n64^m + 4n^3)$ [31]. Despite the exponential complexity, current LP solver implementations are very efficient and capable of solving realistic LP problem formulations. We will demonstrate this in Section 6.

### 5 Iterative Computation

Due to the presence of cache interference, a job may execute longer than $C_k$ on a multicore platform with shared caches. However, a larger execution time may introduce more cache interference, as illustrated in Fig. 11.

In Fig. 11a, if the job of $\tau_k$ executes for $C_k^\prime$, only one job of $\tau_i$ interferes with $\tau_k$. In Fig. 11b, if the job of $\tau_k$ executes for a larger execution time, say $C_k + I^*(C_k^\prime)$, two jobs of $\tau_i$ could possibly interfere with $\tau_k$, which potentially may increase the cache interference exhibited by $\tau_k$. This example suggests an iterative method is needed to find an upper bound on the cache interference.

**Lemma 8.** $I^*(C_k^\prime)$ is non-decreasing with respect to $C_k^\prime$.

**Proof.** If $C_{k'} = C_k + I^*(C_k^\prime)$, then $I^*(C_k^\prime) = I^*(C_k^\prime + I^*(C_k^\prime))$.

According to Lemma 8, given an execution window of $\tau_k$ that is no more than $C_k + I^*(C_k^\prime)$, the cache interference exhibited by $\tau_k$ is not larger than $I^*(C_k^\prime)$. Therefore, $I^*(C_k^\prime)$ is the upper bound on cache interference for $\tau_k$. By definition, $I^*(C_k^\prime) = I^*(C_k^\prime)$.

We now derive the iterative algorithm, called Cache Interference $(\tau, m)$ to compute an upper bound on cache interference for each task $\tau_k \in \tau$.

- Since the constraints of our IP formulation assume the taskset is schedulable, we first assess the schedulability of the taskset assuming no cache interference between each task. Only if all tasks pass schedulability test, the following steps will be taken.
- $C_k^\prime$ is initialized with $C_k$ and an upper bound value on the cache interference $I^*(C_k^\prime)$ is created which is initially set to zero.
- By solving the IP, we compute a new upper bound of the cache interference $I^*(C_k^\prime)$.
- If the new upper bound of cache interference is the same as the old upper bound, the $I^*(C_k^\prime)$ is the final upper bound of $\tau_k$. Otherwise, another round of computing the upper bound on cache interference is performed using the upper bound derived at the previous iteration. The iteration for $\tau_k$ stops either if no update on $I^*(C_k^\prime)$ is possible anymore or if the computed $I^*(C_k^\prime)$ is large enough to make $\tau_k$ unschedulable.
- The previous steps are repeated for every task in $\tau$.

A more formal version of the Cache Interference $(\tau, m)$ algorithm is given by Pseudocode 1. The algorithm returns $I^*$ which includes the upper bounds on cache interference $I^*(C_k^\prime)$ for each task $\tau_k$ and $C^*$ which includes the upper bounds on the execution length $C_k^\prime$ for each $\tau_k$. If $I^*$ and $C^*$ are empty, the taskset is not schedulable.

Since the solution of the IP is non-decreasing with respect to $C_k$ according to Lemma 8 and one termination condition is $C_k^\prime = D_k$, the termination of the iterative algorithm is guaranteed.

Before presenting the final theorem to check the schedulability of the task set, we define the following notations.
We denote $U(\tau_i)$ as task $\tau_i$’s utilization taking shared cache interference into account, $U(\tau_i)$ is defined by

$$U_i = \frac{C_i^*}{T_i}.$$

The utilization of taskset $\tau$, denoted by $U(\tau)$, is defined by

$$U(\tau) = \sum_{i \in \tau} U_i = \sum_{i \in \tau} \frac{C_i^*}{T_i}.$$

We sort all $C_i^*$ in a non-increasing order, and use $\Delta_{C_i^*}^{m-1}$ to denote the sum of the first $(m-1)$ elements in this list, so

$$\Delta_{C_i^*}^{m-1} = \sum_{\text{the (m-1) largest}} C_i^*.$$

For task $\tau_k$, we also define a constant $L_k$ by

$$L_k = \frac{\sum_{i \in \tau_k} C_i^* + \Delta_{C_i^*}^{m-1}}{m - U(\tau)} - S_k. \quad (17)$$

We propose the following Theorem to check the schedulability of the task set.

**Theorem 2.** A task set $\tau$ is schedulable with the EDF$_{up}$ or FP$_{up}$ scheduling policy on a multicore platform composed of $m$ identical cores with shared caches if for each task $\tau_k \in \tau$ and $0 \leq A_k \leq L_k$,

1. $\exists C_i^* \geq C_i$ such that $C_i^* = C_i + I^c(C_i^*)$,
2. $\frac{\Omega_k}{m} + C_i^* < D_k + A_k$.

**Proof.** From (1), $\bar{I}_k^c$ is bounded and $\bar{I}_k^c = I^c(C_k^*)$ according to Lemma 9.

From Lemma 4, $\bar{I}_k^{pre} = \frac{\Omega_k}{m} + C_k^*$. If $A_k \geq 0$, then $\frac{\Omega_k}{m} + C_k^* < D_k + A_k$.

The most $\eta = \max_k \frac{(D_k - C_k)}{(\bar{I}_k^c - \bar{I}_k^{pre})}$ iterations to terminate since $C_i^*$ either stays the same or increases at least with $I^c$ in each iteration. Thus, the complexity of the iterative algorithm to compute the upper bound on cache interference is $O(nm^264^nln4^n)$. The complexity of computing $L_k$, $\Omega_k$ is polynomial. Therefore, the complexity to perform the schedulability test is $O(nm^264^nln4^n)$.

**Pseudocode 2. CheckSchedulability($\tau$, $m$)**

1: Input: Task parameters, number of cores: $m$
2: $I^*, C^* \leftarrow$ CacheInterference($\tau$, $m$)
3: for all $\tau_k \in \tau$ do
4: calculate $L_k$ by Equation (17)
5: for all $A_k \in [0, L_k]$ do
6: $\Omega_k \leftarrow$ calculation of Equation (12) using $C^*$, $A_k$
7: if $\frac{\Omega_k}{m} + C_i^* < D_k + A_k$ then
8: return Unschedulable
9: end if
10: end for
11: end for
12: return Schedulable
6 EXPERIMENTS

In this section, we systematically generate synthetic workloads to evaluate the performance of the proposed schedulability test for $EDF_{up}$ and $FP_{up}$ in terms of acceptance ratio. More specifically, we will quantify the effects of cache interference on the schedulability of the generated tasksets. We will also compare the schedulability performance of $EDF_{up}$ against $FP_{up}$ over randomly generated tasksets.

The experiments have been performed varying i) the probability of two tasks having cache interference on each other: $P$ ($P = 0.1$, 0.2, 0.3 or 0.4), ii) the cache interference factor $IF$ ($IF = 0$, 0.3, 0.6 or 0.9), iii) the number of cores $m$ ($m = 2$, 4 or 8), iv) total task utilization $U_{tot}$ ($U_{tot}$ from 0.1 to $m - 0.1$ with steps of 0.2). Given those three parameters, we have generated 20000 tasksets in each experiment. The number of tasks $n$ in each tasksets is 10, i.e., $n = 10$. As the task generation policies may significantly affect experimental results, we give the policies used in the experiments as follows.

**Task Utilization Generation Policy.** We use Randfixed-sum [32] to generate vectors that consist of $n$ elements and whose components sum to the $U_{tot}$. Each element in the vector is assigned an individual task utilization $U_i$ in the taskset.

**Task Period and WCET Generation Policy.** For each task $t_i$, $T_i$ is uniformly distributed over the interval $[100, 200]$. The WCET of $t_i$ is derived by $C_i = T_i \times U_i$. We consider an implicit deadline task system, which implies that $D_i = T_i$.

**Cache Interference Generation Policy.** The probability of two task having cache interference is $P$. If two tasks $t_k$ and $t_i$ interfere with each other, $I_{k,i}^{wc}$ is generated as $I_{k,i}^{wc} = IF \times min(0.5C_i, 0.5C_k)$.

In each experiment, we measure the number of schedulable tasksets that pass the proposed schedulability test. The acceptance ratios, which is the number of schedulable tasksets divided by the total number of tasksets (20000), are shown in Figs. 12 and 13 for $EDF_{up}$ and $FP_{up}$, respectively.

Fixing $m = 4$, $n = 10$, IF = 0.3, Figs. 12a and 13a illustrate the acceptance ratio with different $P$ for $EDF_{up}$ and $FP_{up}$, respectively. With the same $U_{tot}$, the acceptance ratio for both $EDF_{up}$ and $FP_{up}$ decreases as $P$ increases because a larger $P$ indicates more tasks in the taskset could interfere with each other, which may potentially increase the upper bound on cache interference for each task. Fixing $P$, it can be observed that the acceptance ratio of $EDF_{up}$ is higher than $FP_{up}$ when $U_{tot} \in [1.1, 2.5]$. For example, when $P = 0.2$, IF = 0.3 and $U_{tot} = 1.7$, 60.1 percent of tasksets are schedulable by $EDF_{up}$ while $FP_{up}$ schedules 50.45 percent of the generated tasksets.

Figs. 12b and 13b show the acceptance ratio achieved by $EDF_{up}$ and $FP_{up}$, respectively, for the cases $IF = 0$, 0.3, 0.6, 0.9, fixing $m = 4$, $n = 10$, $P = 0.4$. The red line with $IF = 0$ represents the acceptance ratio when tasks have no cache interference. Evidently, the acceptance ratios with a lower $IF$ are better than those with a larger $IF$. As we increase $IF$ with the same amount, the average acceptance ratio decreases in a slower fashion. However, it does not indicate that a lower bound on the average acceptance ratio is possible since the cache interference gets larger as $IF$ increases, eventually making the interfered tasks unschedulable. Fixing $IF$, it is also clear that the acceptance ratio achieved by $EDF_{up}$ is better than $FP_{up}$ when $U_{tot} \in [0.7, 2.5]$. For example, when $P = 0.4$, IF = 0.6 and $U_{tot} = 1.1$, 66.9 percent of tasksets are schedulable by $EDF_{up}$ while $FP_{up}$ schedules 59.3 percent of the generated tasksets.

Figs. 12c and 13c illustrate the acceptance ratio with respect to the number of cores for $EDF_{up}$ and $FP_{up}$, respectively. In
the two figures, the acceptance ratio for tasks having no cache interference are also plotted. Instead of using \( U_{\text{tot}} \) as horizontal axis, we scale the horizontal axis with \( \frac{U_{\text{tot}}}{m} \) for \( m = 2, 4 \). It is worth noting that an execution platform with fewer cores is more efficient in terms of acceptance ratio than those with more cores. This is due to the fact that the pessimism of the analysis of processor-contention interference and shared cache interference becomes worse when the number of cores increases. However, for processors with different numbers of cores scheduled by EDF\(_{np}\) (or FP\(_{np}\)), the difference in the acceptance ratio of scheduling between the baseline (tasks having no cache interference, \( P = 0 \)) and tasks having cache interference is almost similar.

\[ \text{Average Execution Time} \]

We measured the execution time of running the proposed schedulability test with different task-set scales. The executions are conducted on an Intel Xeon processor using only one core running at 2.4 GHz. On average, it takes 0.13 seconds to check the schedulability of tasksets consisting of 10 tasks, 0.27 seconds for tasksets with 20 tasks, and 0.56 seconds for tasksets with 30 tasks.

7 Conclusion

In this paper, we developed a new schedulability analysis of global scheduling (EDF\(_{np}\) and FP\(_{np}\)) for real-time multicore systems with shared caches. We constructed an integer programming formulation that can be transformed to an integer linear programming formulation to calculate the upper bound on cache interference exhibited by a task during a given execution window. Using this integer formulation, we subsequently proposed an iterative algorithm to obtain an upper bound on the shared cache interference a task may exhibit during one job execution. We derived a new schedulability condition by integrating the upper bound on the cache interference into the schedulability analysis. A set of experiments has been performed using our proposed schedulability analysis to demonstrate the effects of cache interference for a range of different tasksets. We also compared the schedulability performance of EDF\(_{np}\) against FP\(_{np}\) in the presence of cache interference. Our empirical evaluations showed that EDF\(_{np}\) is better than FP\(_{np}\) in terms of tasksets deemed schedulable. As for future work, we plan to extend our schedulability analysis to real-time multicore systems with shared caches that use preemptive task scheduling.

Acknowledgments

The research of this article was supported by Netherlands Organisation for Scientific Research under Project No. 12696 and the University of Amsterdam.

References


Jun Xiao (Member, IEEE) received the BE degree in automation and control engineering from Nanchang University, Nanchang, China, in 2012, the MS degree from the University of Trento and Scuola Superiore Sant’Anna, Pisa, Italy, in 2014, and the PhD degree in computer science from the University of Amsterdam, Amsterdam, The Netherlands, in October, 2019. He is a postdoc researcher with the University of Amsterdam. His research interests include the fields of embedded and real-time systems, schedulability analysis, and computer architecture.

Sebastian Altmeyer (Member, IEEE) received the PhD degree in computer science from Saarland University, Saarbrücken, Germany, in 2012 with a thesis on the analysis of preemptively scheduled hard real-time systems. He is currently an assistant professor (Universitair Docent) with the University of Amsterdam. From 2013 to 2015, he has been a postdoctoral researcher with the University of Amsterdam, and from 2015 to 2016 with the University of Luxembourg. In 2015, he has received an NWO Veni Grant on the timing verification of real-time multicore systems. He has been a program chair of ECRTS 2018 and has served on many conferences on real-time embedded systems, including RTSS, RTAS, RTNS, DATE, and DAC. His research focuses various aspects of the design, analysis and verification of hard real-time systems, with a particular interest in timing verification and multicore architectures.

Andy D. Pimentel (Senior Member, IEEE) received the MSc and PhD degrees in computer science from the University of Amsterdam, Amsterdam, The Netherlands. He is currently an associate professor with the System and Network Engineering Lab, University of Amsterdam. His research interests include system-level modeling, simulation, and exploration of (embedded) multicore and manycore computer systems with the purpose of efficiently and effectively designing and programming these systems. He is a co-founder of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS). He has (co)authored more than 100 scientific publications and is an associate editor of the Elseviers Simulation Modelling Practice and Theory as well as the Springer Journal of Signal Processing Systems. He has served as the general chair of HIPEAC’15, as Local Organization co-chair of ESWaveK15, and as program (vice-)chair of CODES+ISSS in 2016 and 2017. Furthermore, he has served on the TPC of many leading (embedded) computer systems design conferences, such as DAC, DATE, CODES+ISSS, ICCD, ICCAD, FPL, SAMOS, and ESTIMedia.

For more information on this or any other computing topic, please visit our Digital Library at www.computer.org/csdl