High performance reconfigurable computing with cellular automata

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Acronyms and Symbols

ASIC	Application specific integrated circuit
BRAM	Block RAM
CA	Cellular automata
CB	Compute block
CE	Compute engine
CLB	Configurable logic block
COTS	Commercial off the shelf
DDR	Double data rate
DRAM	Dynamic RAM
DSP	Digital signal processor
FDTD	Finite difference time domain
FPGA	Field programmable gate array
HPC	High performance computing
HPRC	High performance reconfigurable computing
LBM	Lattice Boltzmann method
LGCA	Lattice Gas Cellular Automata
LUT	Lookup table
MLUPS	Million lattice-site updates per second
PCI	Peripheral component interconnect
PE	Processing element
PMC	PCI mezzanine card
RAM	Random access memory
SDRAM	Synchronous dynamic RAM
SRAM	Static RAM

T_{pc}	CA execution time on a PC
T_{fpga}	CA execution time on a FPGA
T_{ft}	CA execution time on a FPGA-enabled PC
T_{pre}	Time to pre-process a CA lattice by a host machine
T_{pos}	Time to post-process a CA lattice by a host machine
T_s	Time to download a CA lattice from the host PC to the FPGA on-board memory
T_r	Time to upload a CA lattice from the FPGA on-board memory to the host PC

T_{fo}	Total overhead time ($= T_{pre}+T_s+T_r+T_{pos}$)
p	Number of PEs running in a FPGA
k	Number of CA cell FPGA reads in parallel from source memory bank
N	Number of CA lattice cells
x	Number of CA lattice columns
y	Number of CA lattice rows
n	Number of compute blocks (pipeline depth) within a FPGA
g	Number of CA iterations
w	Buffer size within a compute block
F	Number of FPGAs
τ_{r}	FPGA time to read k-cells from the on-board memory bank
τ_{w}	FPGA time to write k-cells to a on-board memory bank
τ_{c}	FPGA time to update a cell
τ_{d}	Host PC time to download a cell to a FPGA on-board memory
τ_{m}	Time to update a boundary cell across two neighbouring FPGAs
T_{c}	FPGA execution time for a compute bound computation
T_{i}	FPGA execution time for an I/O bound computation
T_1	FPGA execution time to compute a single CA iteration
T_2	Execution time to compute a single CA iteration using a dual FPGA-enabled system
T_{f}	Execution time to compute a CA iteration using a F FPGA-enabled PC
T_{F}	Execution time to compute a CA iteration using a F FPGA-enabled PC cluster